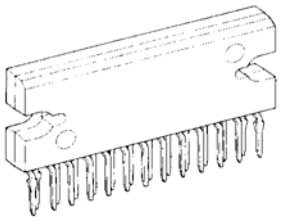
THB6064H

PWM Chopper-Type bipolar
Stepping Motor Driver IC

THB6064H



Weight:
HZIP25-P-1.27: 9.86 g (typ.)

The THB6064H is a PWM chopper-type sinusoidal micro-step bipolar stepping motor driver IC.
It supports 8 kind of excitation modes and forward/reverse mode and is capable of low-vibration, high-performance drive of 2-phase bipolar type stepping motors using only a clock signal.

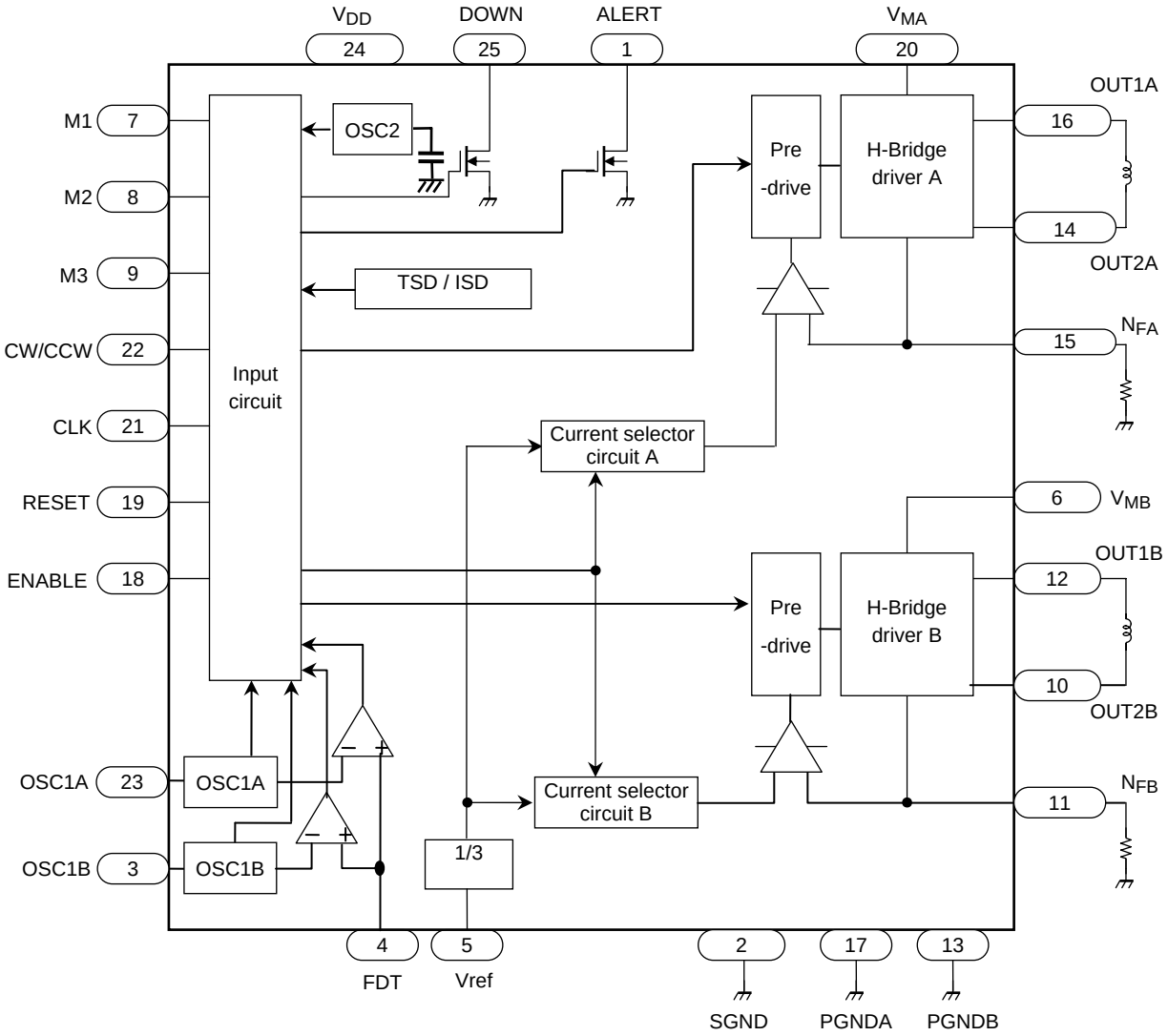
Features

- Single-chip bipolar sinusoidal micro-step stepping motor driver
- Uses high withstand voltage BiCD process:
  Ron (upper, lower) = 0.4 Ω (typ.)
- Forward and reverse rotation control available
- Selectable phase drive (1/2,1/8,1/10, 1/16, 1/20, 1/32, 1/40, 1/64 step)
- High output withstand voltage: VDSS = 50 V
- High output current: I_{OUT} = 4.5 A (peak)
- Packages: HZIP25-P-1.27
- Output monitor pins (DOWN / ALERT)
- Equipped with reset and enable pins
- Built-in thermal shutdown(TSD) and over-current detection(ISD) circuit

*: Since this product has a MOS structure, it is sensitive to electrostatic discharge. These ICs are highly sensitive to electrostatic discharge. When handling them, please be careful of electrostatic discharge, temperature and humidity conditions.

The THB6064H is a Sn-Ag plated product including Pb.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230˚C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245˚C
   *dipping time = 5 seconds
   *the number of times = once
   *use of R-type flux

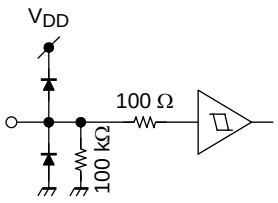
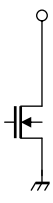
Block Diagram



Pin Functions

Pin No.	I/O	Symbol	Functional Description	Remark
1	Output	ALERT	TSD / ISD monitor pin	
2	—	SGND	Signal ground	
3	—	OSC1B	B channel Capacitor connection pin for off-time setting	
4	Input	FDT	Voltage input pin for mixed decay ratio setting	
5	Input	Vref	Voltage input for 100% current level	
6	Input	V_{MB}	Motor power supply pin for B channel	
7	Input	M1	Excitation mode setting input pin	Built-in pull-down resistor
8	Input	M2	Excitation mode setting input pin	Built-in pull-down resistor
9	Input	M3	Excitation mode setting input pin	Built-in pull-down resistor
10	Output	OUT2B	B channel output 2	
11	—	N_{FB}	B channel output current detection pin	Connect external resistor
12	Output	OUT1B	B channel output 1	
13	—	PGNDB	Power ground	
14	Output	OUT2A	A channel output 2	
15	—	N_{FA}	B channel output current detection pin	Connect external resistor
16	Output	OUT1A	A channel output 1	
17	—	PGNDA	Power ground	
18	Input	ENABLE	Enable signal input pin	H: Enable, L: all output off
19	Input	RESET	Reset signal input pin	
20	Input	V_{MA}	Motor power supply pin for A channel	
21	Input	CLK	CLK pulse input pin	
22	Input	CW/CCW	Forward/reverse control pin	L: Forward, H: reverse
23	—	OSC1A	A channel Capacitor connection pin for off-time setting	
24	Input	V_{DD}	Control side power pin.	
25	Output	DOWN	CLK frequency monitor pin	

<Terminal circuits>

Input pins (M1, M2, M3, CLK, CW/CCW, ENABLE and RESET)	Output pins (DOWN, ALERT)
	

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{DD}	6	V
	$V_{MA/B}$	50	
Output current	$I_{O\ (PEAK)}$	4.5(Note 1)	A/phase
Drain current (TSD, DOWN)	I_{TSD}	1	mA
	I_{DOWN}		
Input voltage	V_{IN}	5.5	V
Power dissipation	P_D	5 (Note 2)	W
		43 (Note 3)	
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note 1: T = 100ms

Note 2: Ta = 25°C, No heat sink.

Note 3: Ta = 25°C, with infinite heat sink (HZIP25).

Operating Range (Ta = –30 to 85°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	$V_{MA/B}$	$V_{MA/B} \geqslant V_{DD}$	4.5	—	42	V
Output current	I_{OUT}	—	—	—	4	A
Input voltage	V_{IN}	—	0	—	5.5	V
	V_{ref}	—	0.5	—	3	
Clock frequency	f_{CLK}	—	—	—	100	kHz
OSC frequency	f_{OSC}	—	—	—	100	kHz

Electrical Characteristics (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Control circuit

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	M1, M2, M3, CW/CCW, CLK, RESET, ENABLE	2.0	—	V_{DD}	V
	Low	$V_{IN\ (L)}$		−0.2	—	0.8	
Input hysteresis voltage		V_H		—	400	—	mV
Input current		$I_{IN\ (H)}$	M1, M2, M3, CW/CCW, CLK, RESET, ENABLE V_{IN} = 5.0 V	—	55	(80)	μA
		$I_{IN\ (L)}$	V_{IN} = 0 V	—	—	1	
VDD supply current		I_{DD1}	Output open, RESET: H, ENABLE: H M1:L, M2:L, M3:L (1/2-step mode)	—	3	(7)	mA
		I_{DD2}	RESET: L, ENABLE: H	—	2	(7)	
		I_{DD3}	RESET: L, ENABLE: L	—	2	(7)	
V_M supply current		I_{M1}	RESET: H/L, ENABLE: L	—	0.5		mA
		I_{M2}	RESET: H/L, ENABLE: H	—	1		
Vref input circuit	Input current	$I_{IN(ref)}$	Vref=3.0V	—	—		μA
	Divider ratio	V_{ref}/V_{NF}	Maximum current : 100%		3		—
Mixed-decay comparator	Input current	$I_{IN(FDT)}$		—	—		μA
	Input voltage range	V_{FDT}	Slow decay mode	3.5	—	V_{DD}	V
			Mixed decay mode(Peak voltage)	(2.9)	3.1	(3.3)	
			Mixed decay mode(Bottom voltage)	(0.9)	1.1	(1.3)	
			Fast decay mode	—	—	0.8	
Minimum CLK pulse width		$t_{W\ (CLK)}$		—	10	—	μs
Output residual voltage		V_{OL} DOWN	I_{OL} = 1 mA	—	—	0.5	V
		V_{OL} ALERT					
TSD operation temperature(Note)		TSD	(Design target value)	—	170	—	°C
TSD hysteresis (Note)		TSDhys	(Design target value)	—	40	—	°C
Off time（Note）		T_{OFF1A} , T_{OFF1B}	C_{OSC1A}, C_{OSC1B} = 1000pF (Design target value)	16	23	35	μ sec
Oscillation circuit for CLK monitor	Detection CLK frequency	fdetect	using built-in capacitor	(0.75)	1.5	(3.0)	Hz

Note: Pre-shipment testing is not performed.

Output Block

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Output ON resistor		$Ron_H + Ron_L$	I_{OUT} = 4 A	—	0.4	(0.6)	Ω
Output transistor switching characteristics		t_r	R_L = 2 Ω, V_{NF} = 0 V, C_L = 15 pF	—	0.1	—	μs
		t_f		—	0.1	—	
Output leakage current	Upper side	I_{LH}	V_M = 50 V	—	—	1	μA
	Lower side	I_{LL}		—	—	1	

Description of Functions

1. Excitation Settings

You can use the M1, M2 and M3 pin settings to configure four different excitation settings. (The default is 2-phase excitation using the internal pull-down.)
Please be sure to set up 'Low' or 'High' always at M1, M2 and M3 terminals.
Although M1、M2 and M3 terminals have built-in pull-down resistors, please do not keep M1、M2 and M3 terminals open.

Input			Mode (Excitation)
M1	M2	M3	
L	L	L	1/2
L	L	H	1/8
L	H	L	1/10
L	H	H	1/16
H	L	L	1/20
H	L	H	1/32
H	H	L	1/40
H	H	H	1/64

2. Function

When the ENABLE signal goes Low level, it sets an OFF on the output. The output changes to the Initial mode shown in the table below when the RESET signal goes Low level. In this mode, the status of the CLK and CW/CCW pins are irrelevant.

Input				Output Mode
CLK	CW/CCW	RESET	ENABLE	
↑	L	H	H	CW
↑	H	H	H	CCW
X	X	L	H	Initial mode
X	X	X	L	Z

X: Don't care

3. Initial Mode

When RESET is used, the phase currents are as follows.

Excitation Mode	A Phase Current	B Phase Current
1/2 step	100%	0%
1/8 step	100%	0%
1/10 step	100%	0%
1/16 step	100%	0%
1/20 step	100%	0%
1/32 step	100%	0%
1/40 step	100%	0%
1/64 step	100%	0%

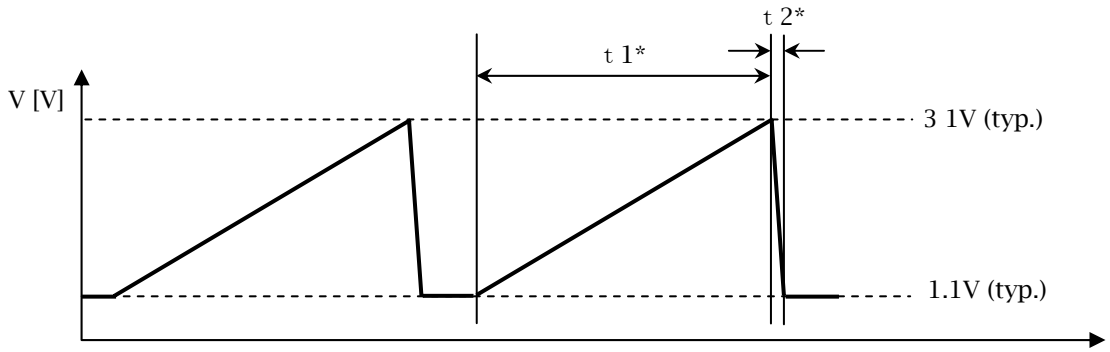
4. OSC circuit

Oscillating waveform of chopping wave is generated by connecting the capacitor (C_{OSC1A} and C_{OSC1B}) between OSC1A , OSC1B and GND terminal.
The fixed off-time (T_{OFF1A} and T_{OFF1B}) can be calculated by the following equation:

$$T_{OFF1A} \fallingdotseq C_{OSC1A} \div (4.4 \times 10^{-5}) \quad [sec]$$
$$T_{OFF1B} \fallingdotseq C_{OSC1B} \div (4.4 \times 10^{-5}) \quad [sec]$$

(A gap is between actual values because this is an approximate expression.)

The recommended value for T_{OFF1A} and T_{OFF1B} is from 15 μ s to 35 μ s.
The recommended value for C_{OSC1A} and C_{OSC1B} is from 680pF to 1000pF.



) t1 : t2*=30:1

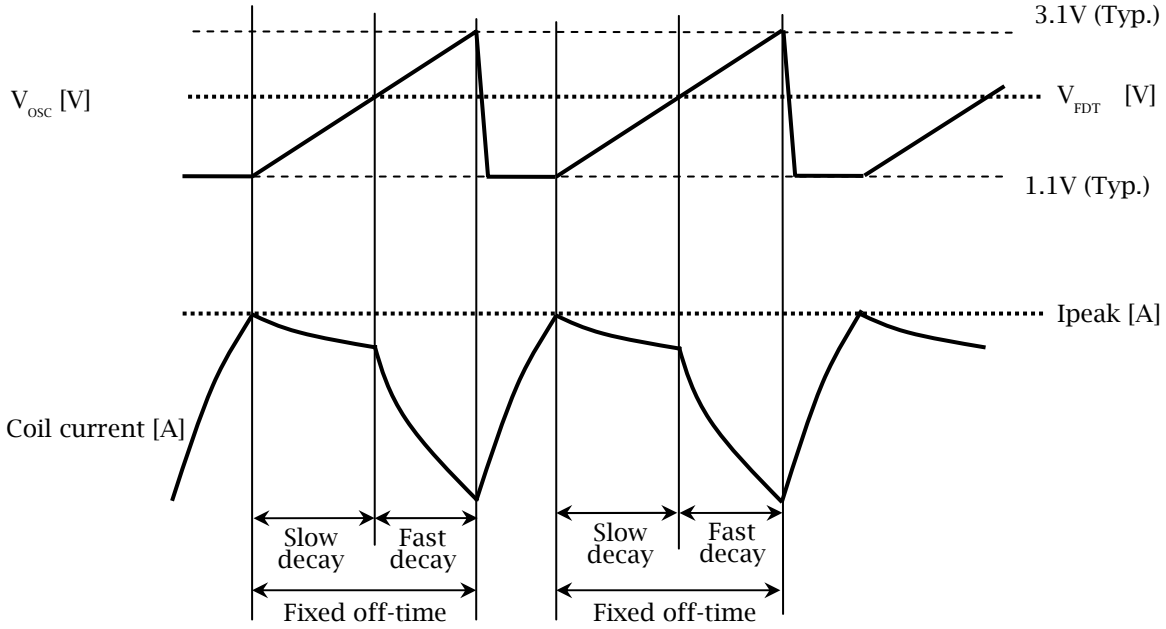
5. Decay mode

By comparing the input voltage of FDT terminal and the OSC chopping wave, the rate of the fast-decay time and the slow-decay time in the mixed-decay mode can be set up.

V_{FDT} [V]	Decay mode
3.5 < V_{FDT} < V_{DD}	Slow decay
1.1 < V_{FDT} < 3.1	Mixed-decay
0 < V_{FDT} < 0.8	Fast decay

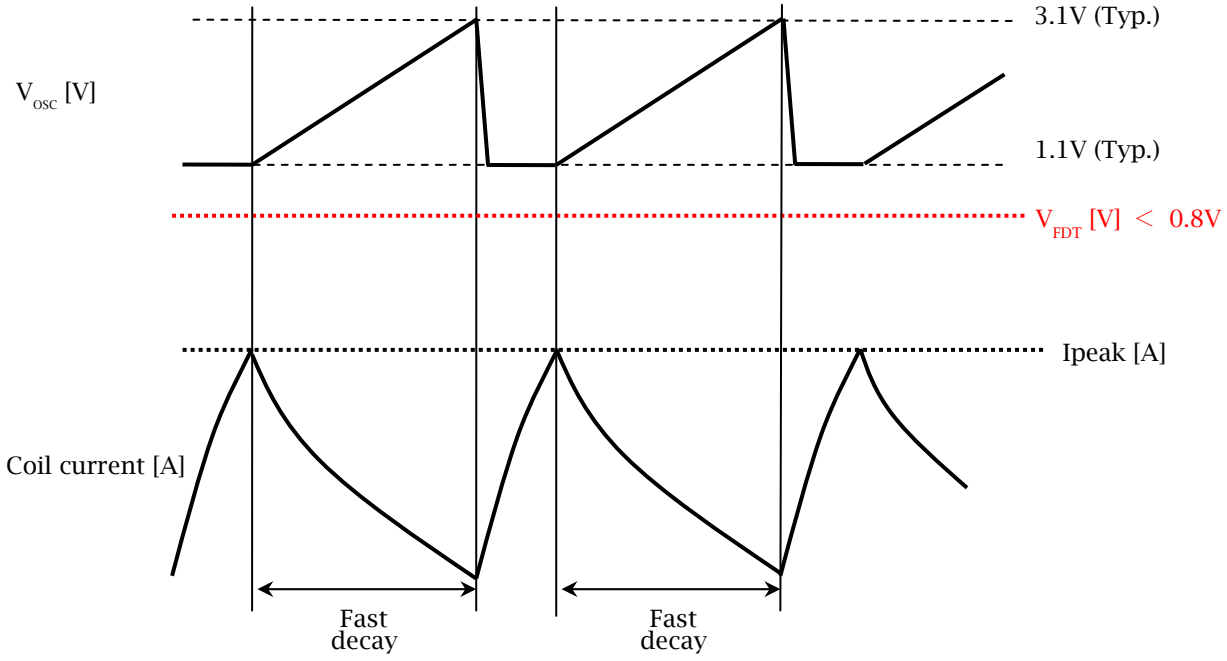
1) Mixed-decay

When FDT is from 1.1V to 3.1V, it moves to the mixed-decay mode.
PWM turns on and the coil current increases in synchronizing with the timing of the peak voltage of Vosc. When the coil current reaches the setup current, PWM turns off and it moves to the slow-decay mode. And the coil current decreases. After that, it switches from the slow-decay mode to the fast-decay mode in the timing that Vosc reaches VFDT and the motor current decreases. Then, in the timing that Vosc reaches peak voltage, PWM turns on again and the coil current increases.
There is reverse-current protection in fast decay mode by zore-detection.



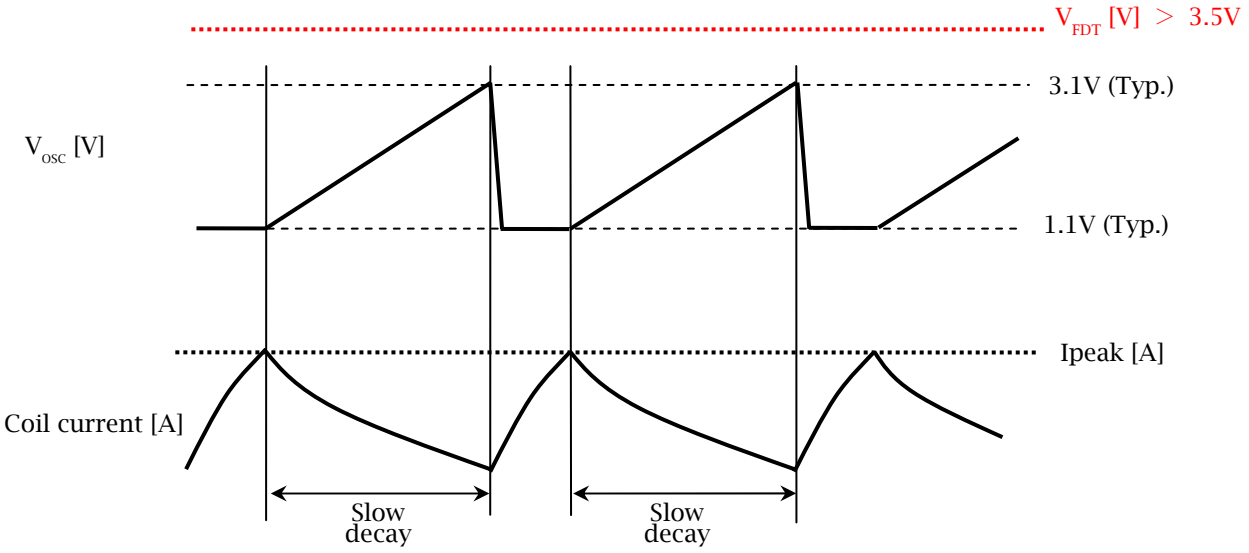
2) Fast-decay

When VFDT is less than 0.8V, it moves to the fast-decay mode.
When the coil current reaches set up value, it moves to the fast–decay mode and the coil current decreases.
In synchronizing with the peak voltage of Vosc, PWM turns on and the coil current increases.
There is reverse-current protection in fast decay mode by zore-detection.



3) Slow-decay

When VFDT is more than 3.5V, it moves to the slow-decay mode.
When the coil current reaches set up value, it moves to the slow-decay mode and the coil current decreases.
In synchronizing with the peak voltage of Vosc, PWM turns on and the coil current increases.



6. 100% current Settings (Current Value)

100% current value is determined by Vref inputted from external part and the external resistance for detecting output current.
Vref is doubled 1/3 inside IC, and compared with VRS.

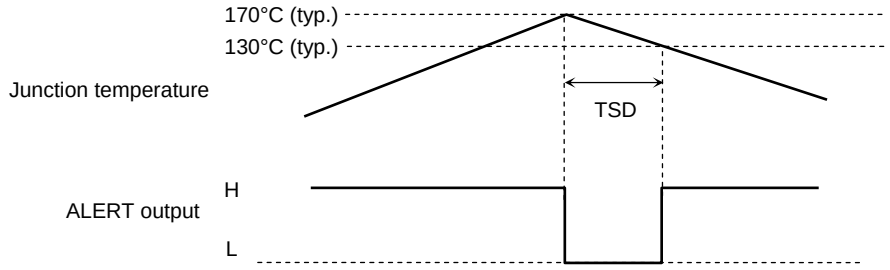
Io(100%) = Vref x 1/3 x 1/Rs

The average current is lower than the calculated value because this IC has the method of peak current detection.

7. Thermal Shut-Down circuit

The IC incorporates a thermal shutdown circuit. When the junction temperature (T_j) reaches 170˚C (typ.), the output power MOSFETs are turned off.
The output power MOSFETs are turned on automatically.
The IC has 40˚C of temperature hysteresis.

TSD = 170˚C (target spec) (Note)
ΔTSD = 40˚C (target spec) (Note)

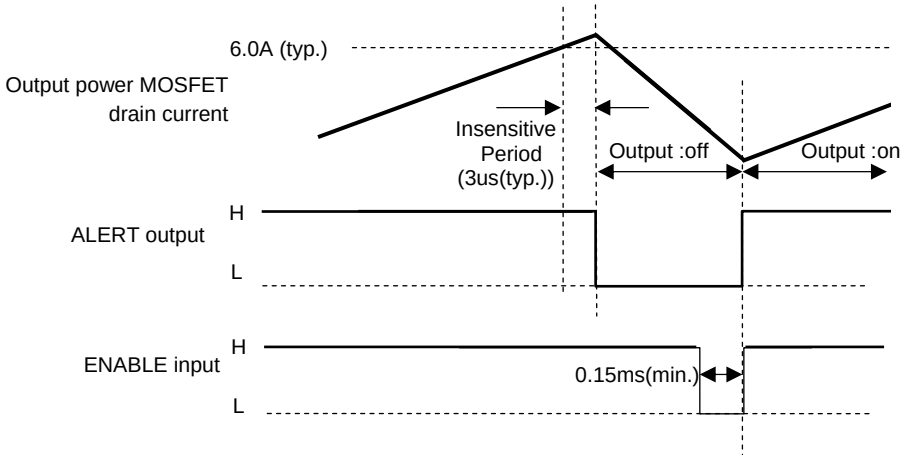


Note: Pre-shipment testing is not performed.

8. ISD (Over current detection)

Current that flow through output power MOSFETs are monitored individually. If over-current is detected in at least one of all output power MOSFETs, all output power MOSFETs are turned off then this status is kept until ENABLE signal is input. Target value in design is 6A and dispersion of ±1.5A should be considered.

ISD = 6A (typ.) ±1.5A (Note)



Note: Pre-shipment testing is not performed.

9. Low voltage detection (UVLO) circuit

Outputs are shutoff by operating at 3.9V (Typ.) of V_{DD} or less.
It has a hysteresis of 0.1V(Typ.) and recover to output when V_{DD} reaches 4.0V(Typ.).

- **The state of internal IC when the ULVO circuit is driving**

The states of the internal IC, outputs, and the IC after recovery correspond to the enable mode.

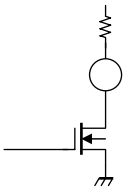
10. ALERT output

ALERT pin outputs the state of TSD and ISD. When TSD or ISD circuit operates, ALERT pin state changes from high impedance to low.

V_{ALERT} = 0.5V (max.) at 1mA

TSD	ISD	ALERT pin
Under TSD opeartion	Under ISD opeartion	Low
Normal	Under ISD operation	
Under TSD opeartion	Normal	
Normal	Normal	Z

Open-drain connection



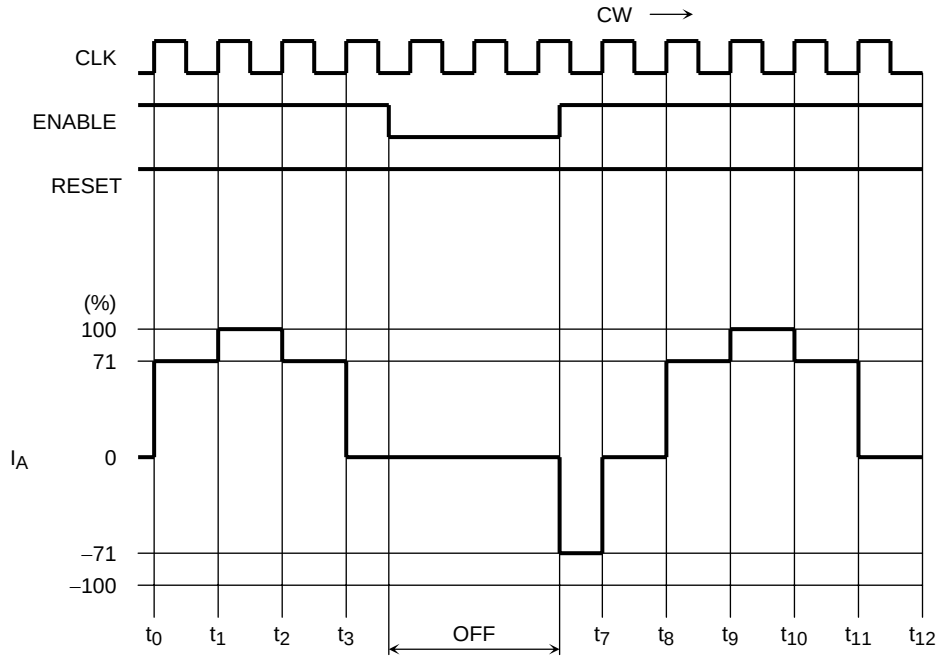
11. DOWN

When IC detects CLK frequency less than 1.5Hz, output of DOWN pin turns to LOW.

Pin State	DOWN
Low	$f_{CLK} \leqq 1.5Hz$
Z	$f_{CLK} > 1.5Hz$

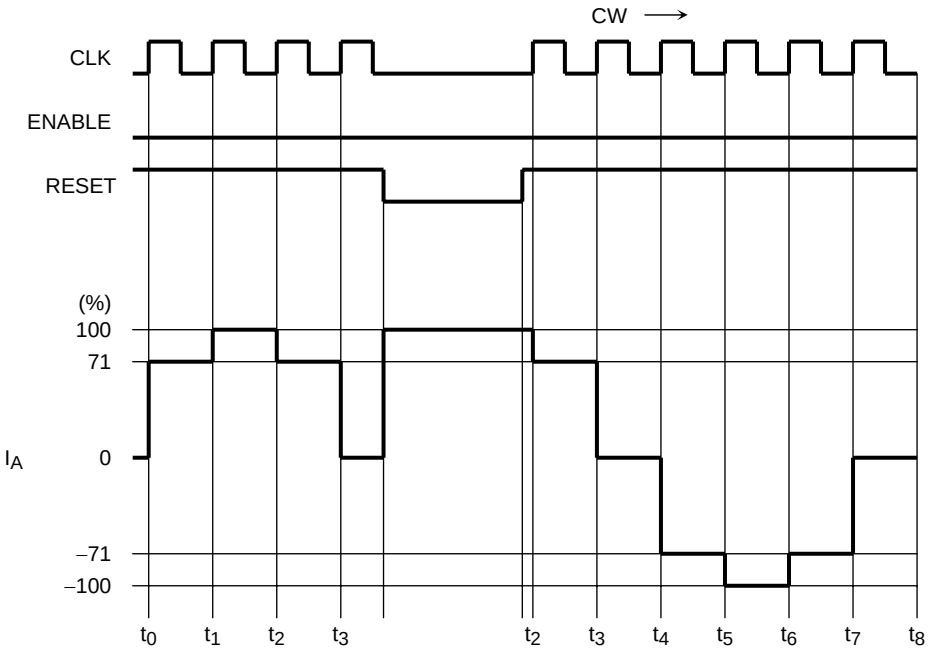
Relationship between Enable, RESET and Output (OUT)

Ex-1: ENABLE 1/2-step mode(M1: L, M2: L, M3: L)



The ENABLE signal at Low level disables only the output signals. Internal logic functions proceed in accordance with input clock signals and without regard to the ENABLE signal. Therefore output current is initiated by the timing of the internal logic circuit after release of disable mode.

Ex-2: RESET 1/2-step mode (M1: L, M2: L, M3: L)

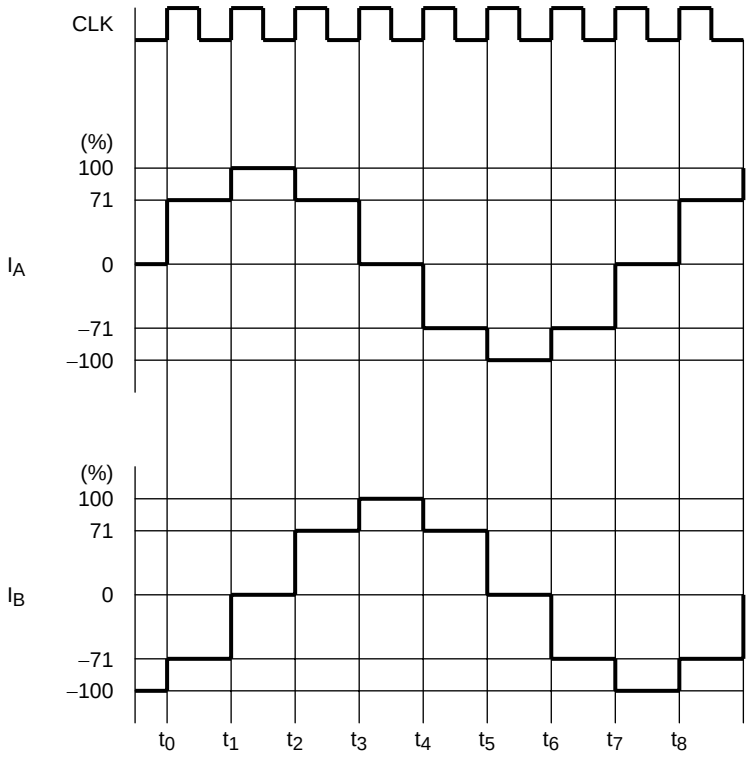


When the RESET signal goes Low level, output goes Initial state (Initial state: A Channel output current is 100%).

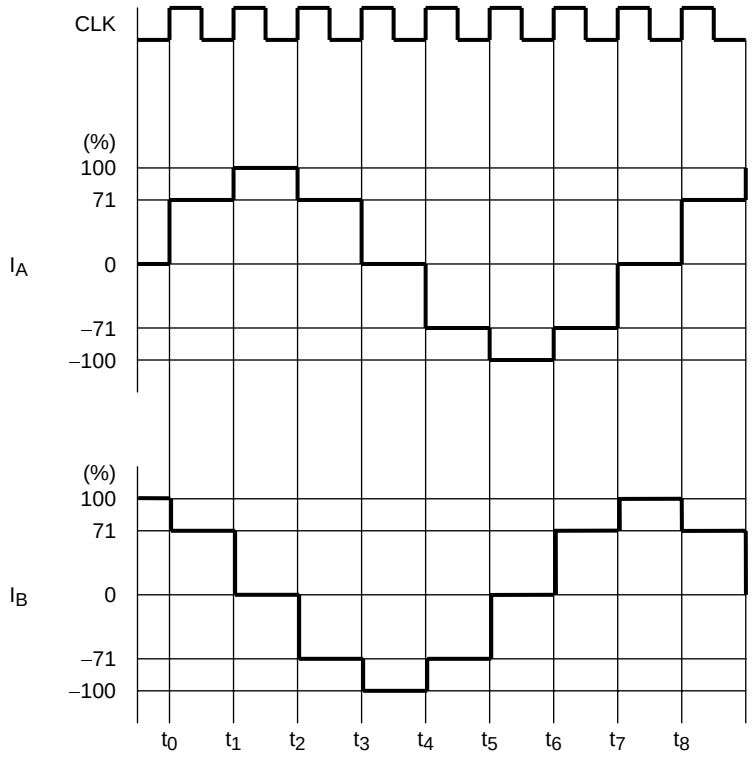
Once the RESET signal returns to High level, output continues from the next state after Initial from the next raise in the Clock signal.

Sequences of output waveform I_A/I_B at each excitation mode

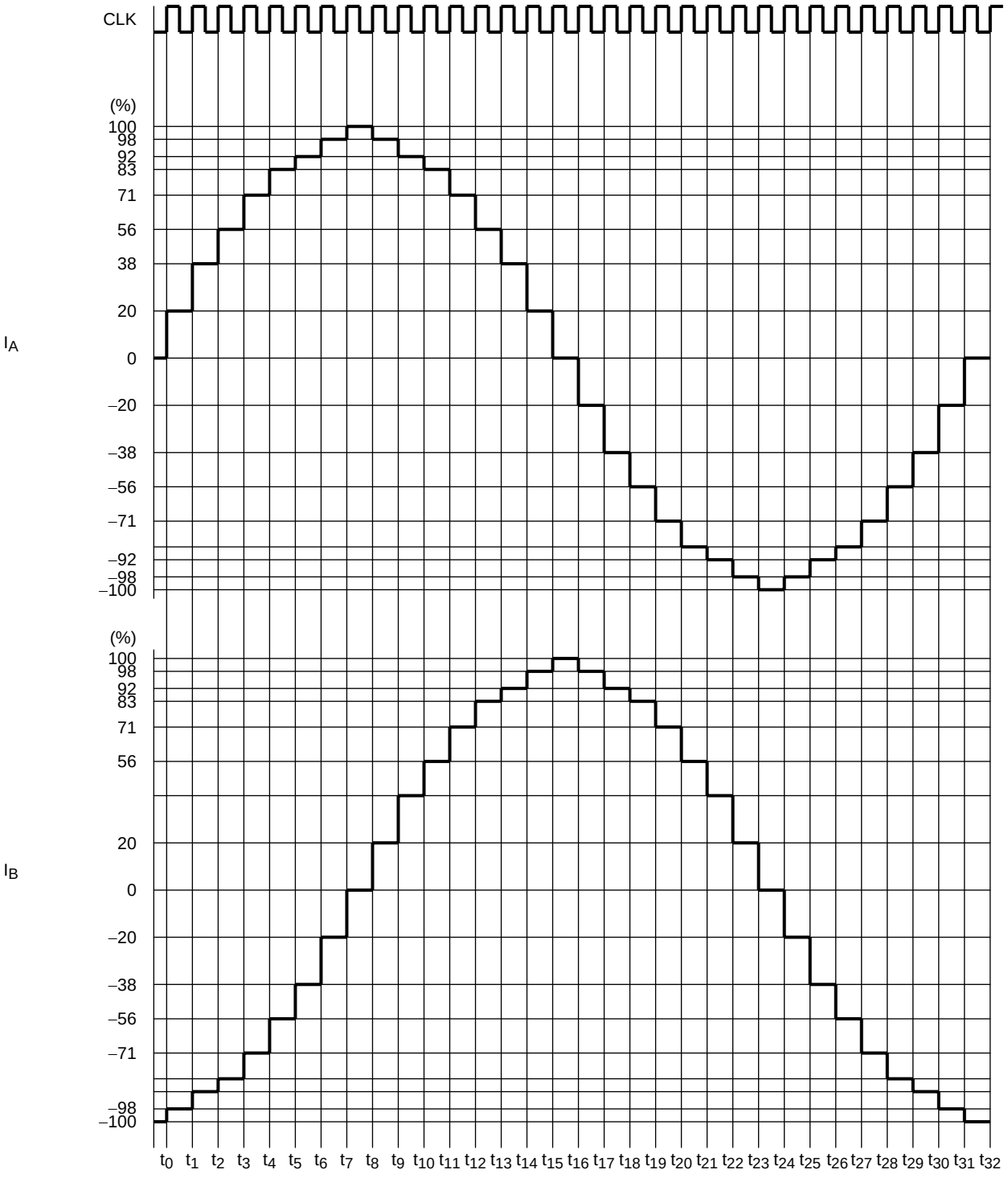
1/2-step Excitation Mode (M1: L, M2: L, M3: L, CW Mode)



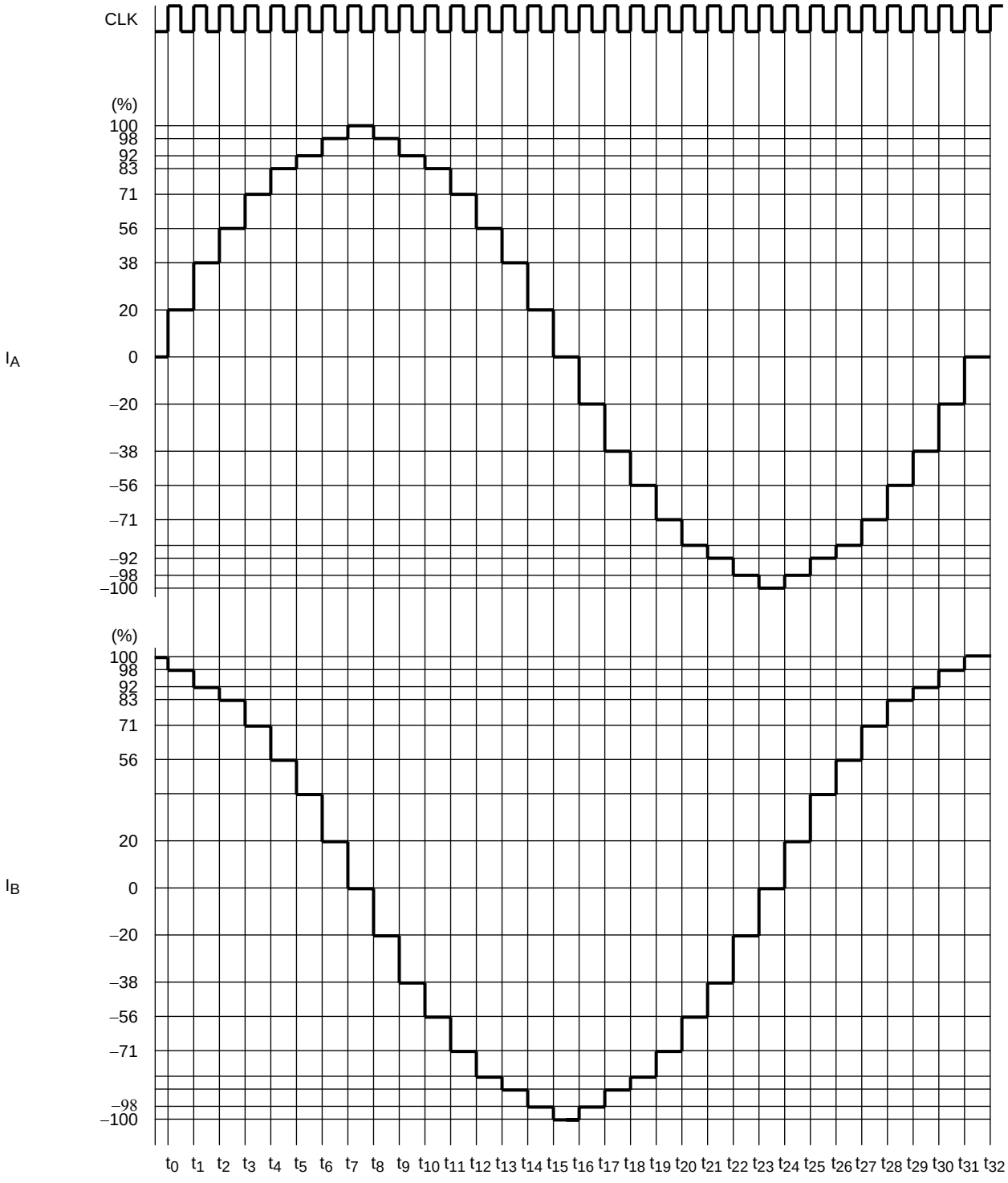
1/2-step Excitation Mode (M1: L, M2: L, M3: L, CCW Mode)



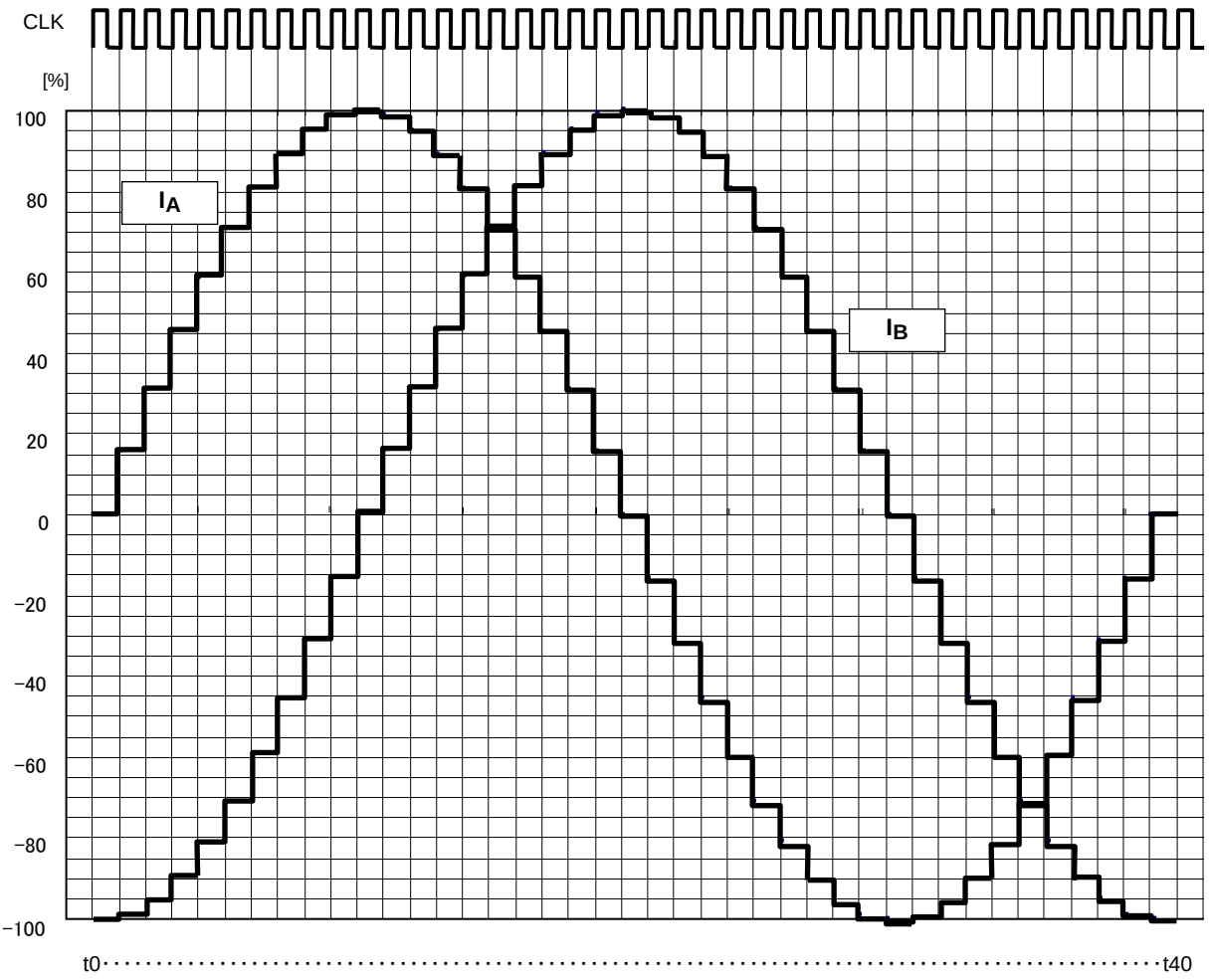
1/8-Step Excitation Mode (M1: H, M2: L, M3: H, CW Mode)



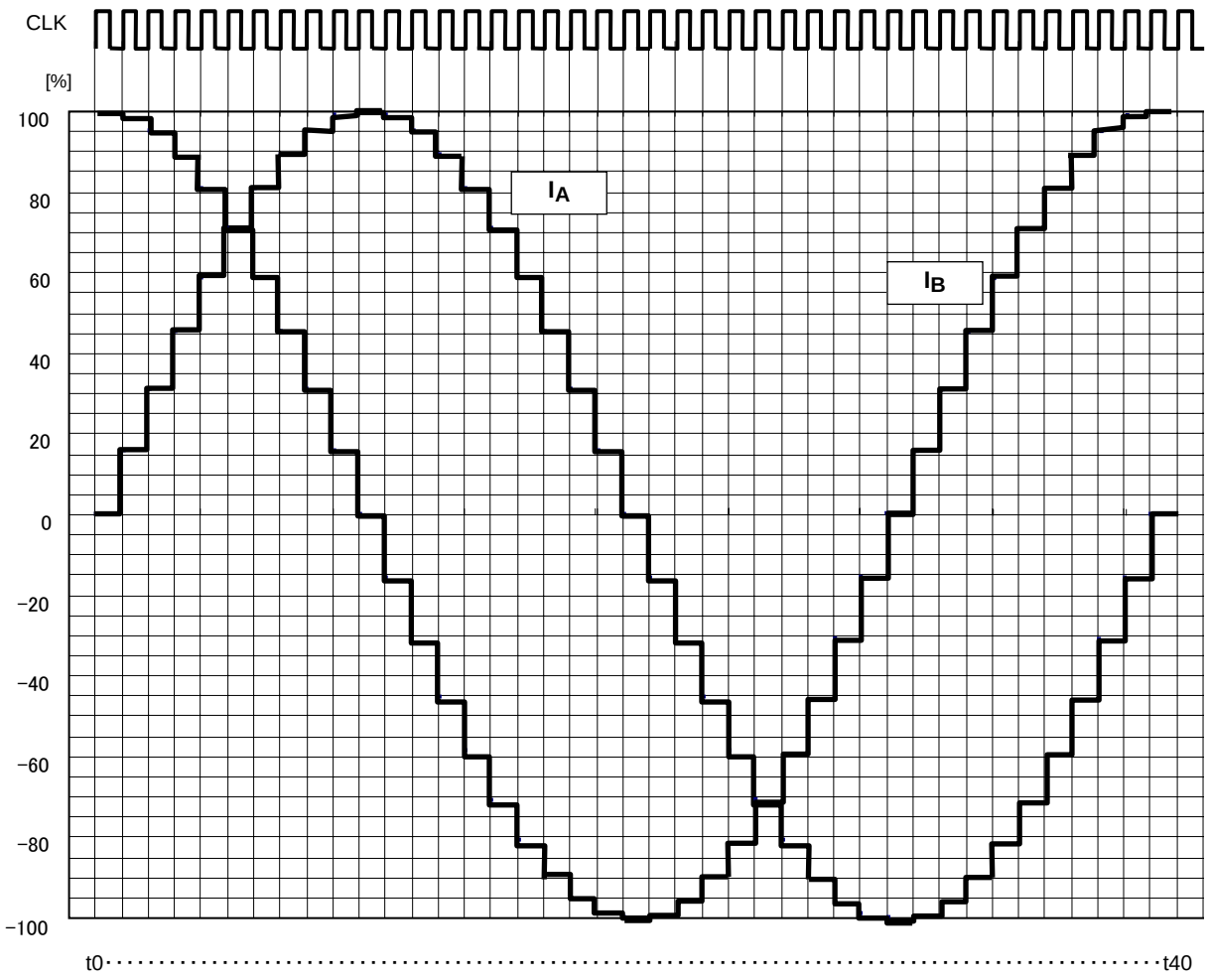
1/8-Step Excitation Mode (M1: H, M2: L, M3: H, CCW Mode)



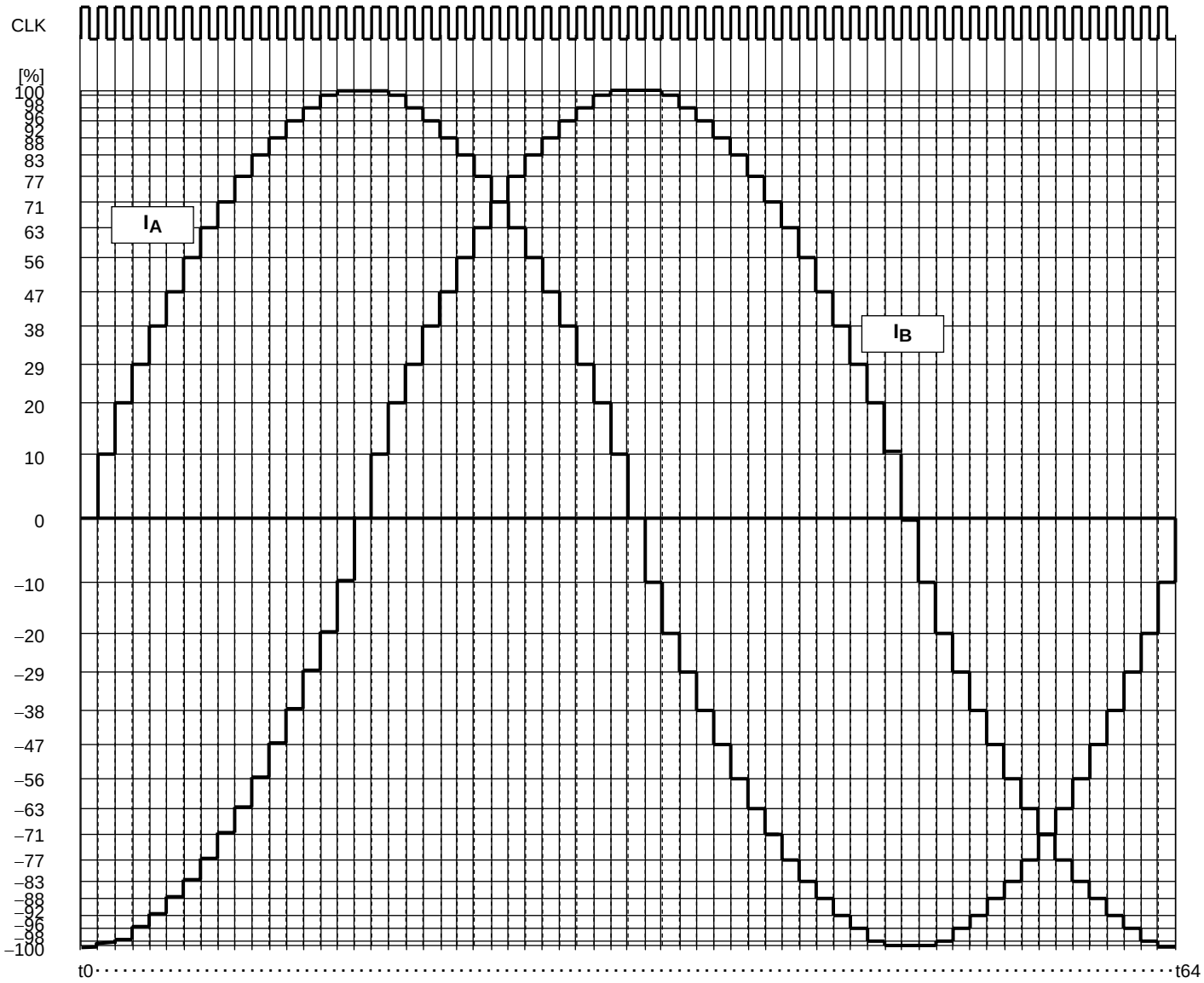
1/10-step Excitation Mode (M1: L, M2: H, M3: L, CW Mode)



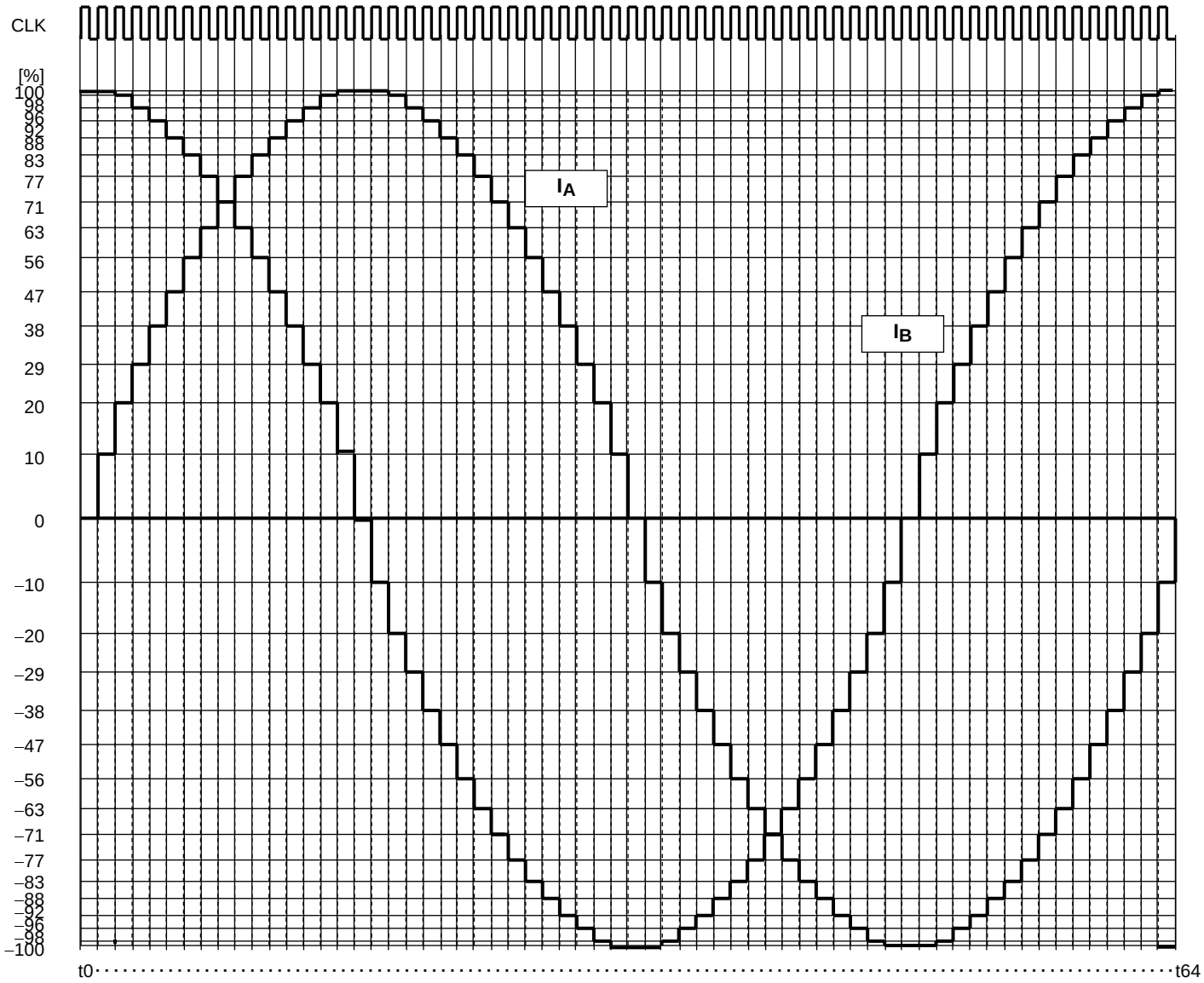
1/10-step Excitation Mode (M1: L, M2: H, M3: L, CCW Mode)



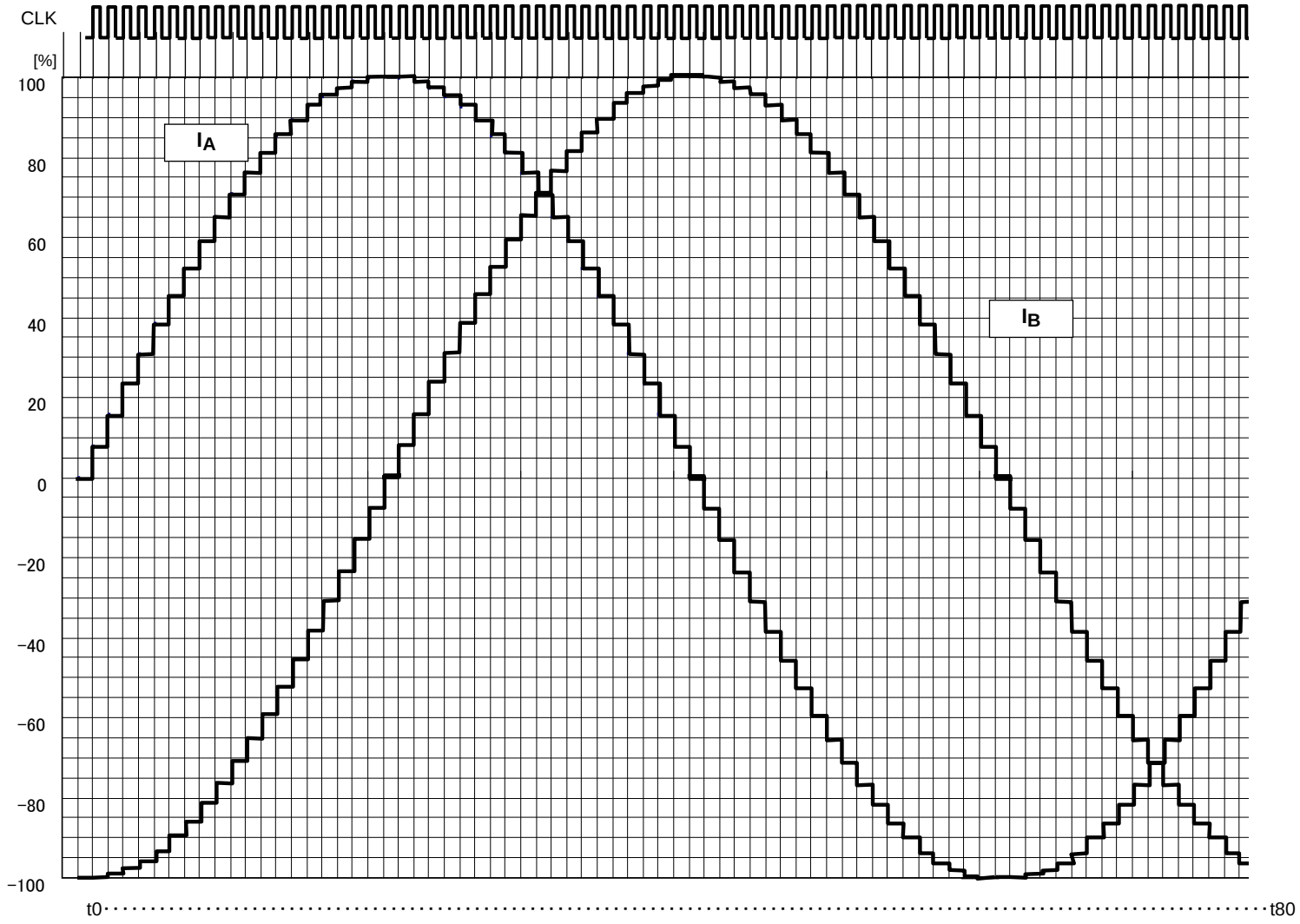
1/16-step Excitation Mode (M1: L, M2: H, M3: H, CW Mode)



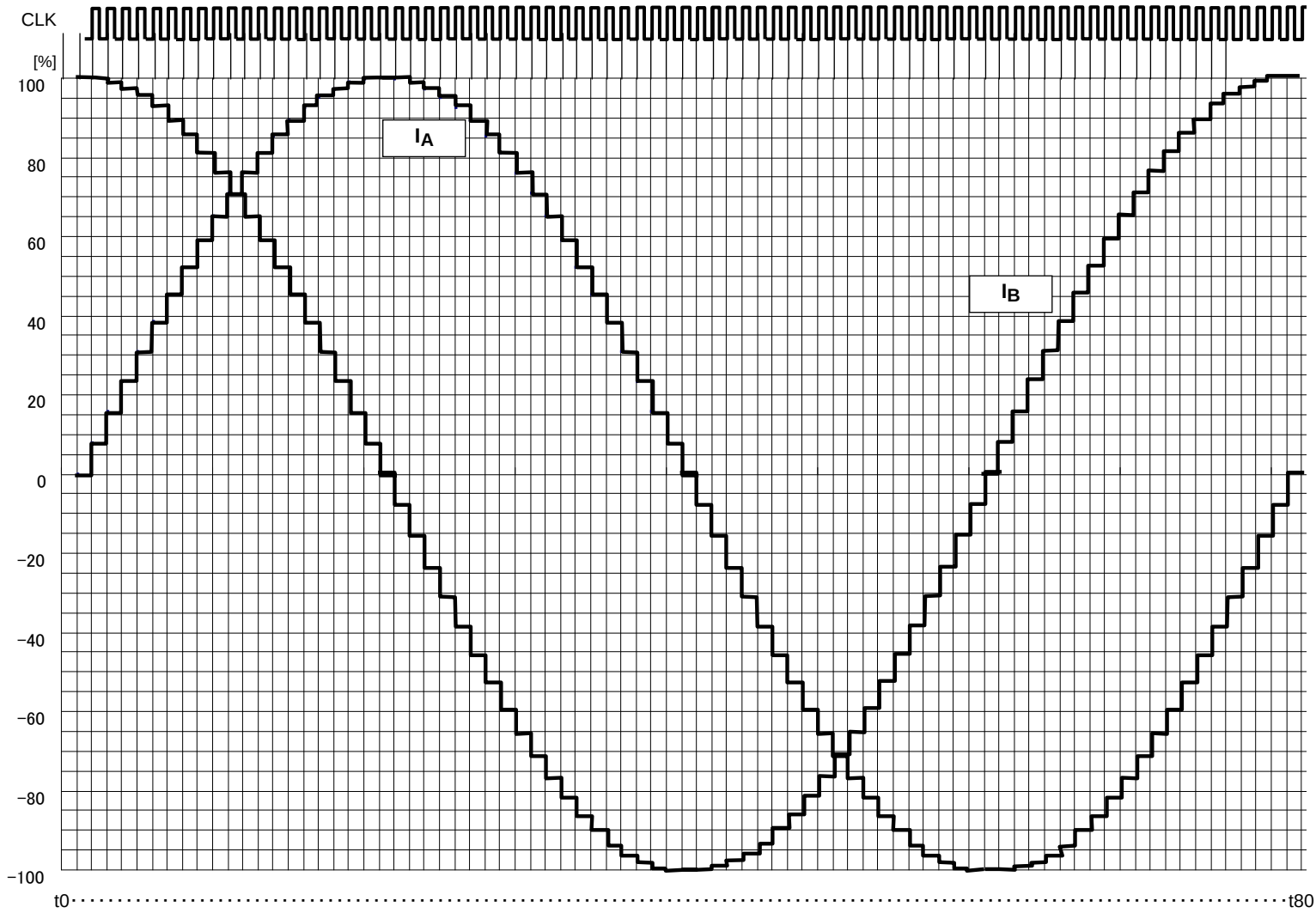
1/16-step Excitation Mode (M1: L, M2: H, M3: H, CCW Mode)



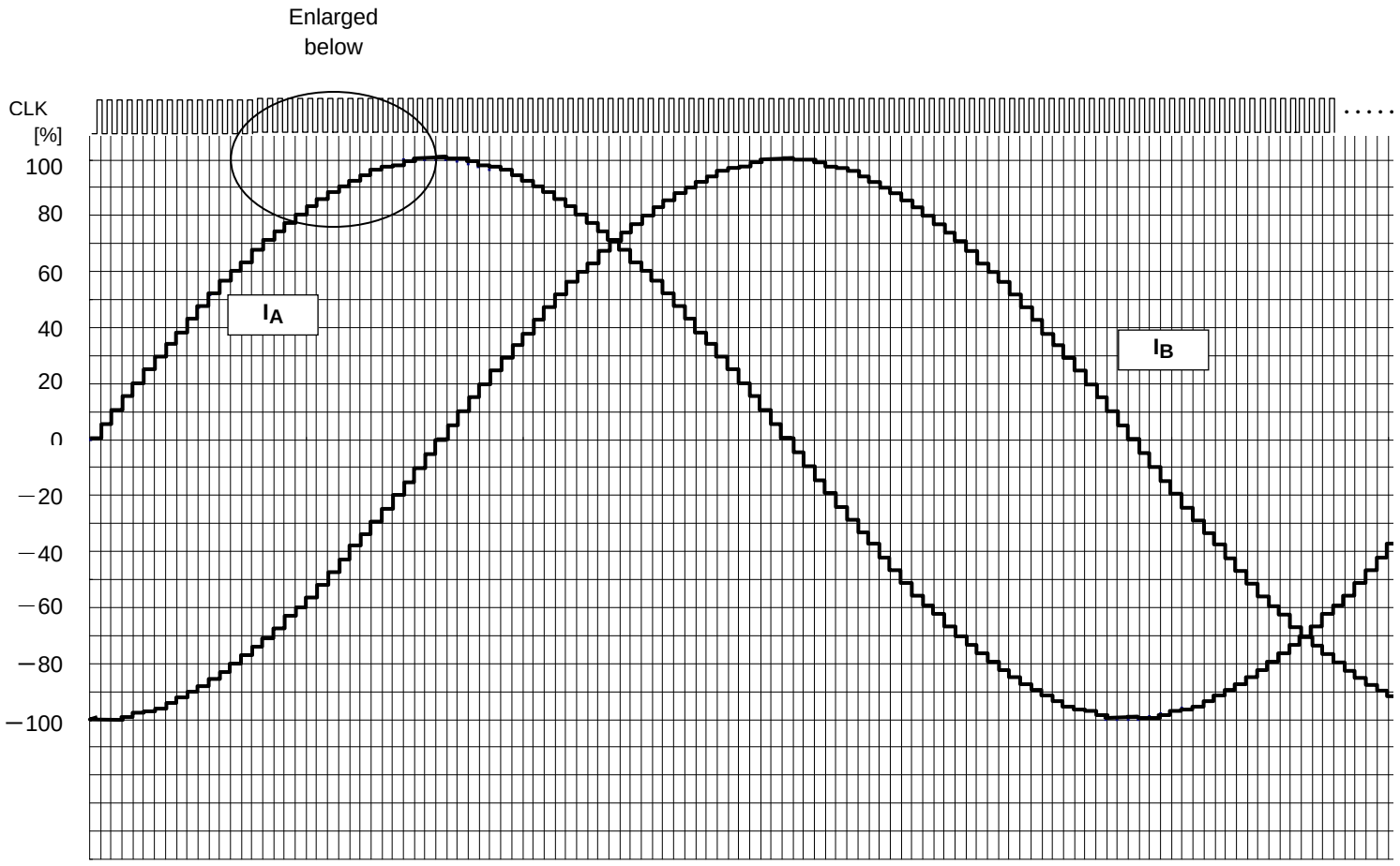
1/20-step Excitation Mode (M1: H, M2: L, M3: L, CW Mode)

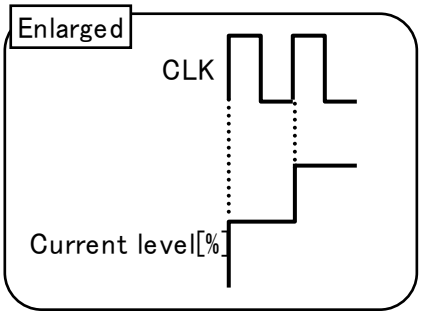


1/20-step Excitation Mode (M1: H, M2: L, M3: L, CCW Mode)

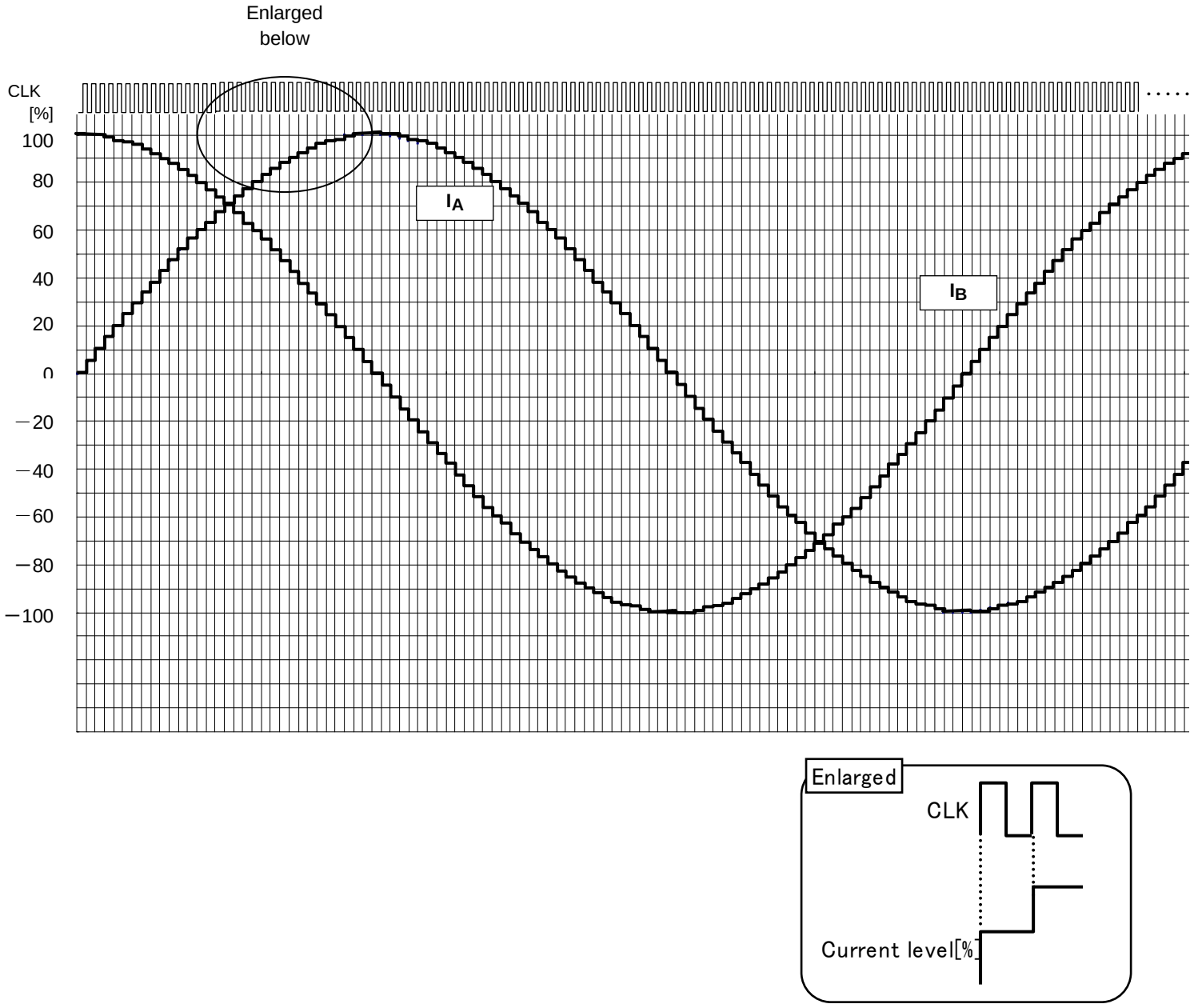


1/32-step Excitation Mode (M1: H, M2: L, M3: H, CW Mode)

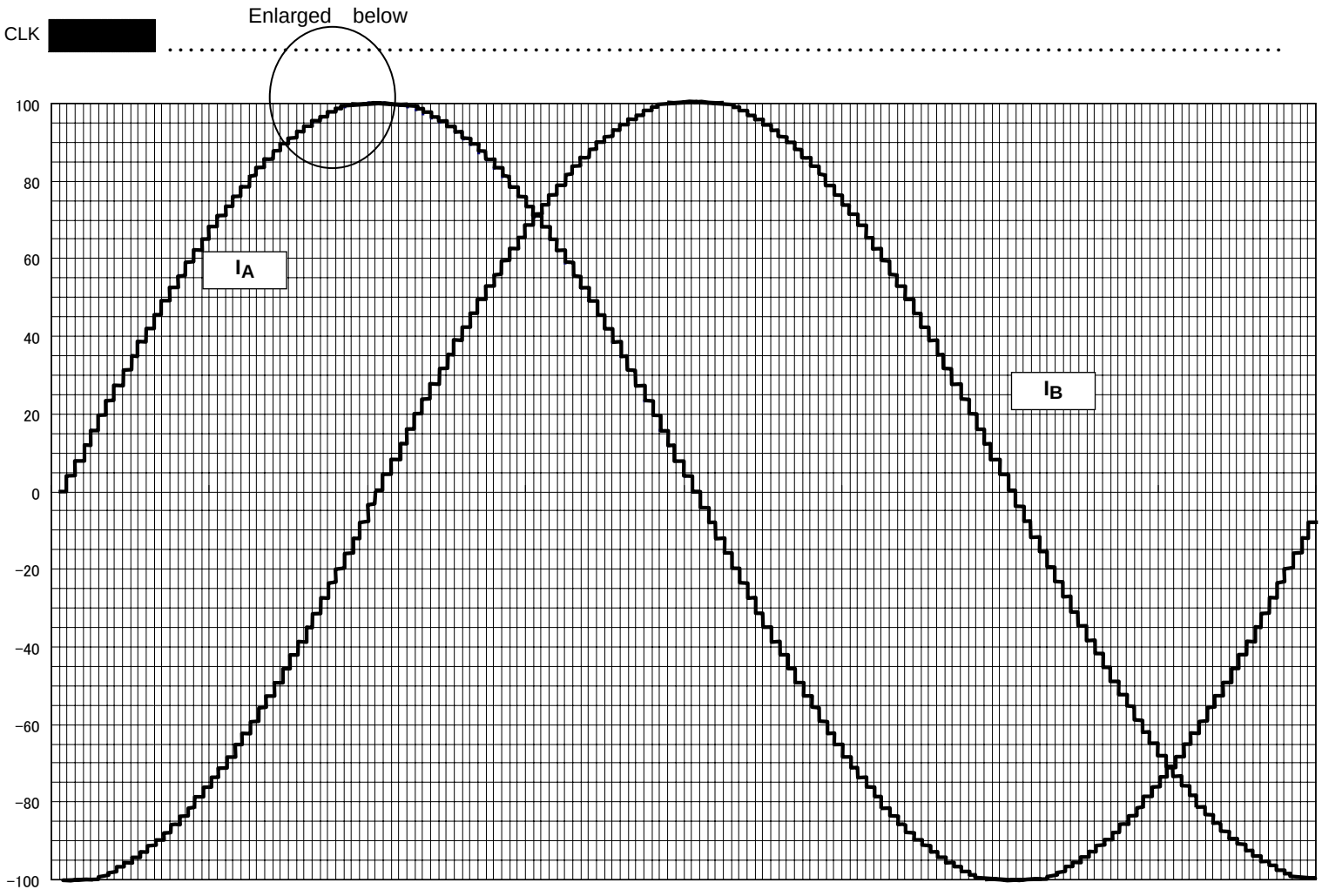


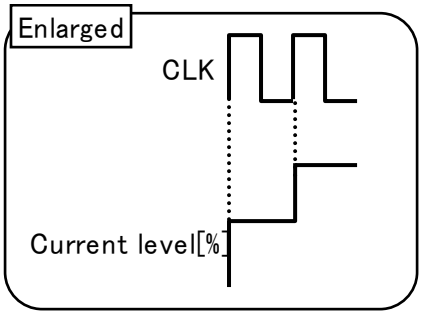


1/32-step Excitation Mode (M1: H, M2: L, M3: H, CCW Mode)

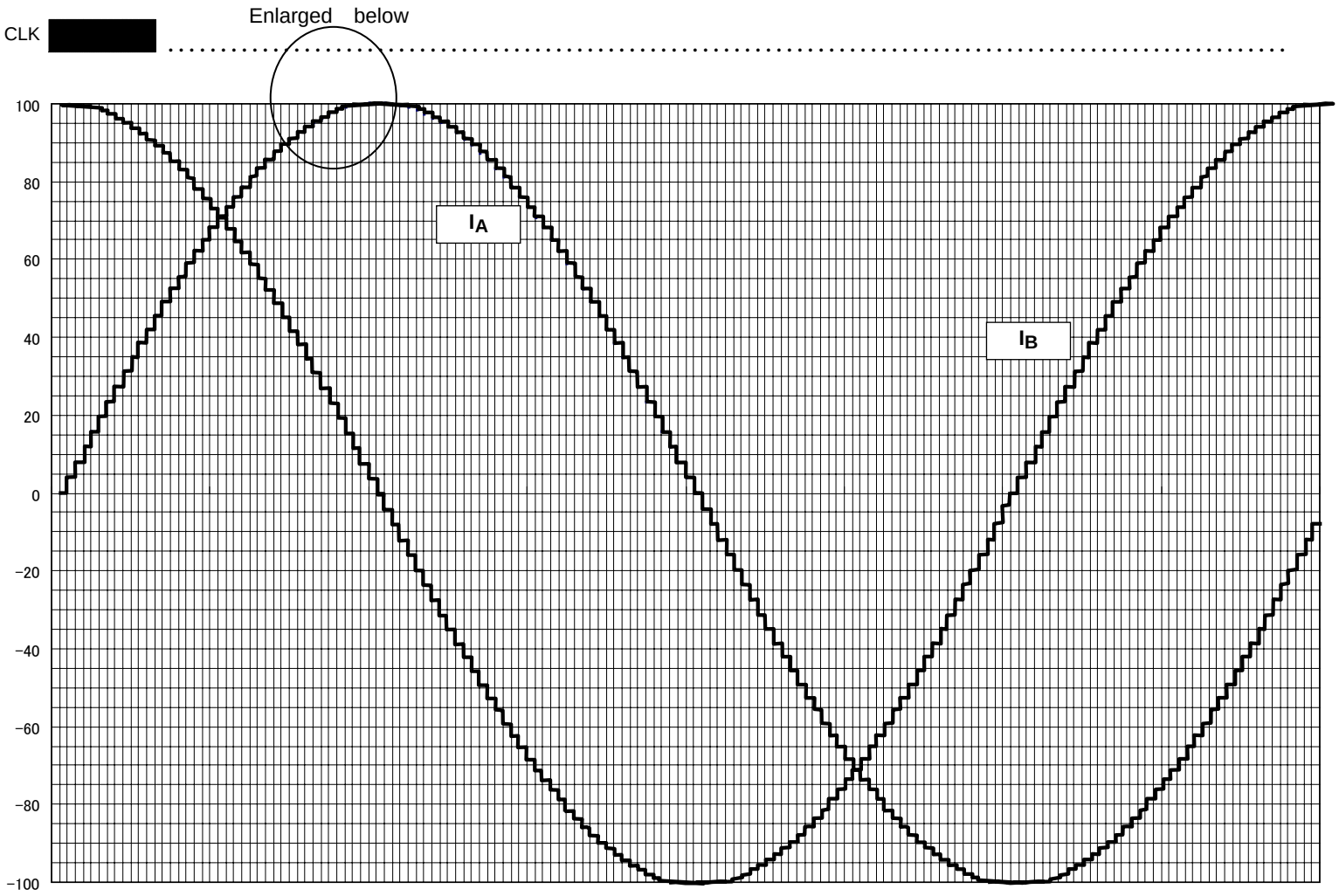


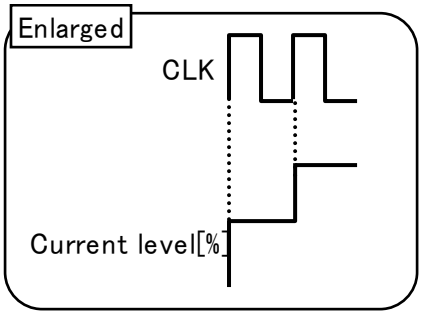
1/40-step Excitation Mode (M1: H, M2: H, M3: L, CW Mode)



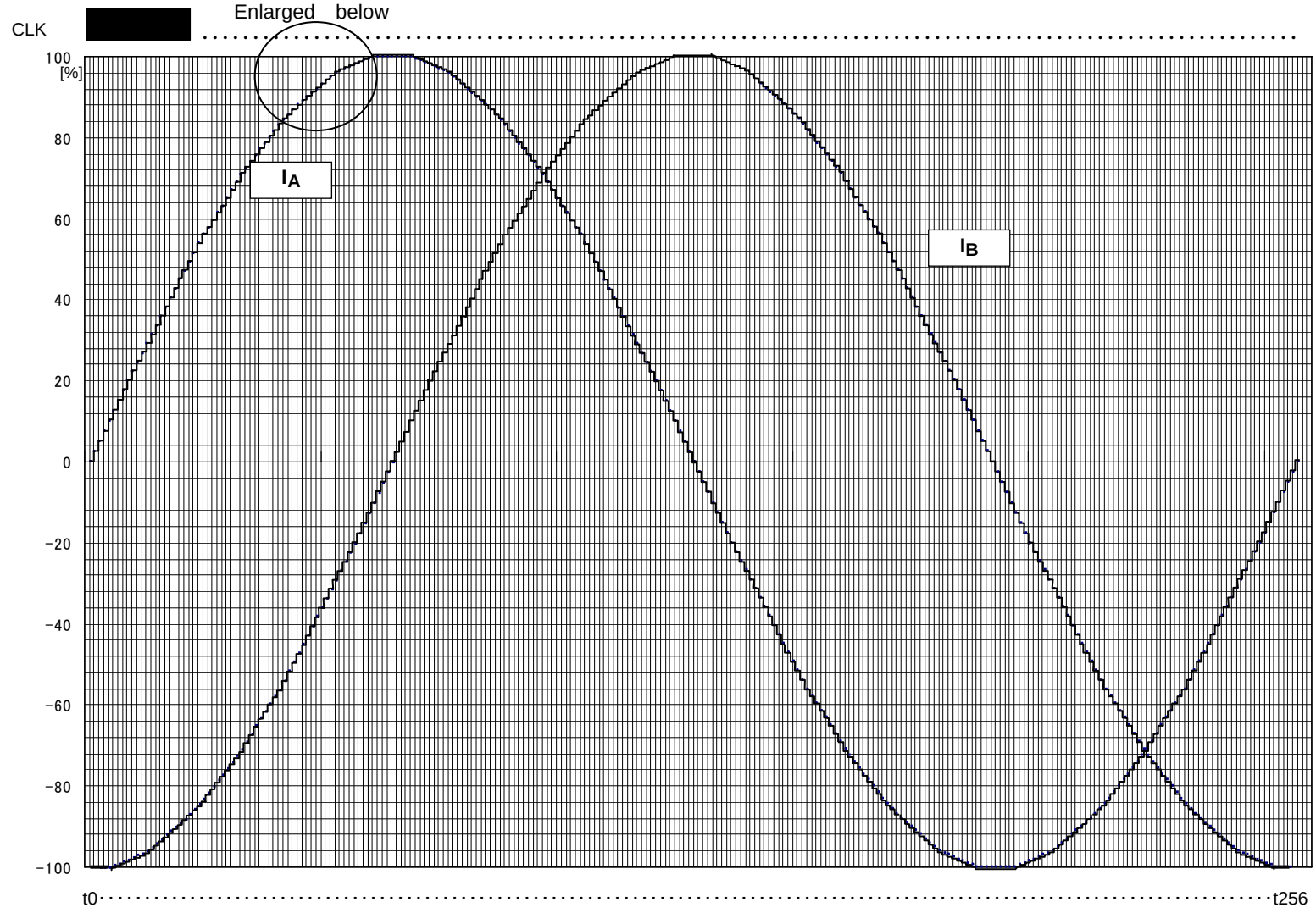


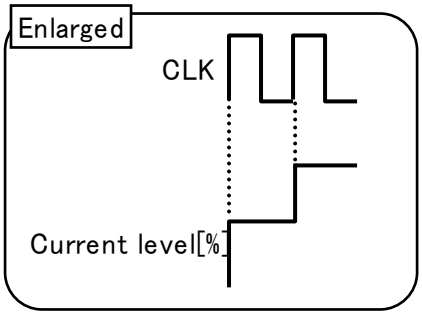
1/40-step Excitation Mode (M1: H, M2: H, M3: L, CCW Mode)



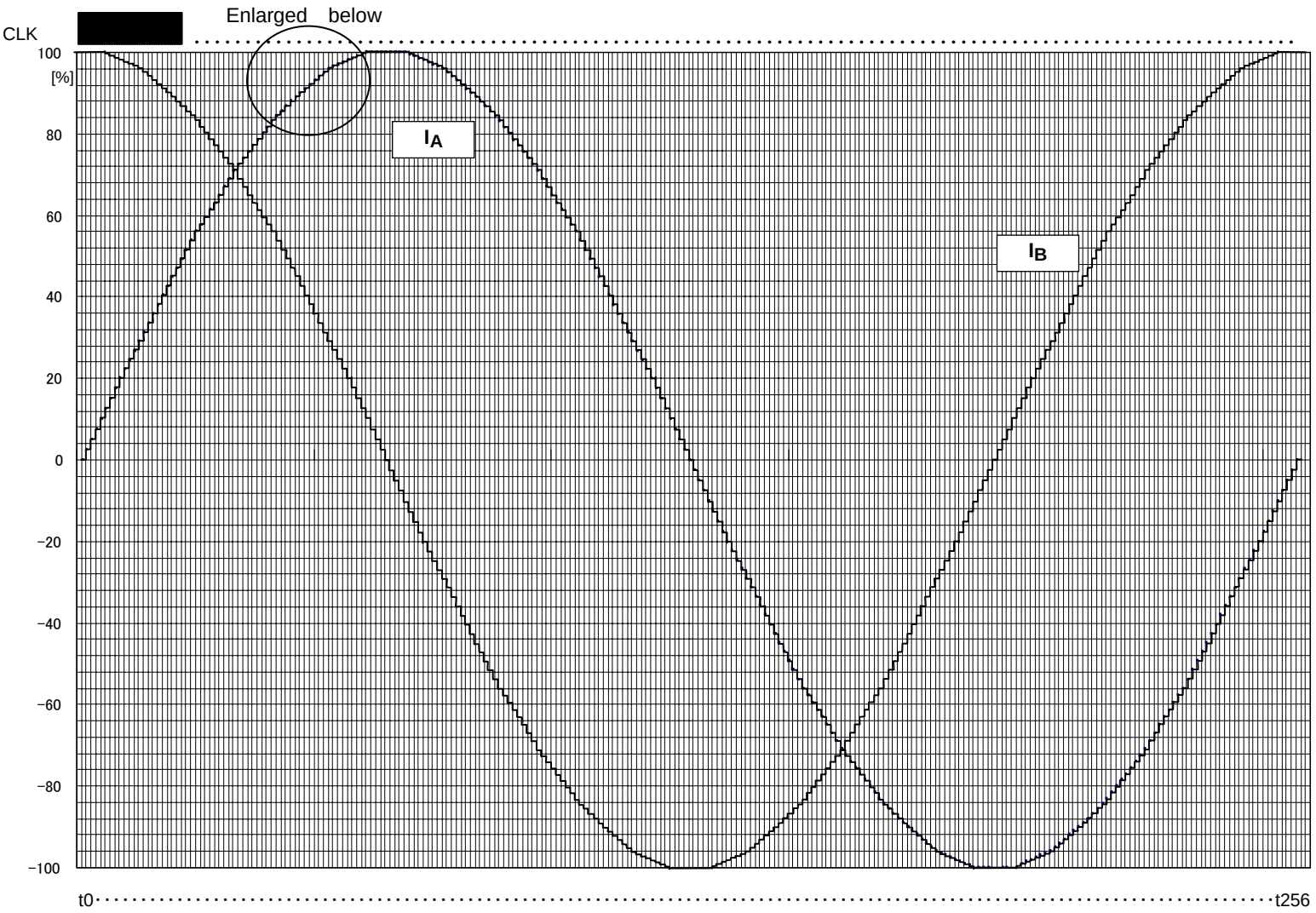


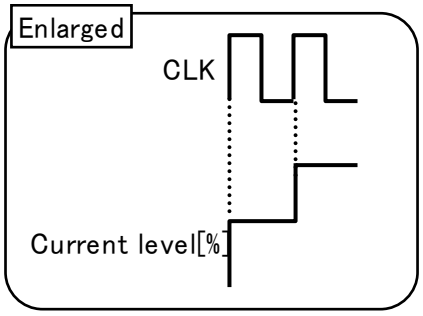
1/64-step Excitation Mode (M1: H, M2: H, M3: H, CW Mode)





1/64-step Excitation Mode (M1: H, M2: H, M3: H, CCW Mode)





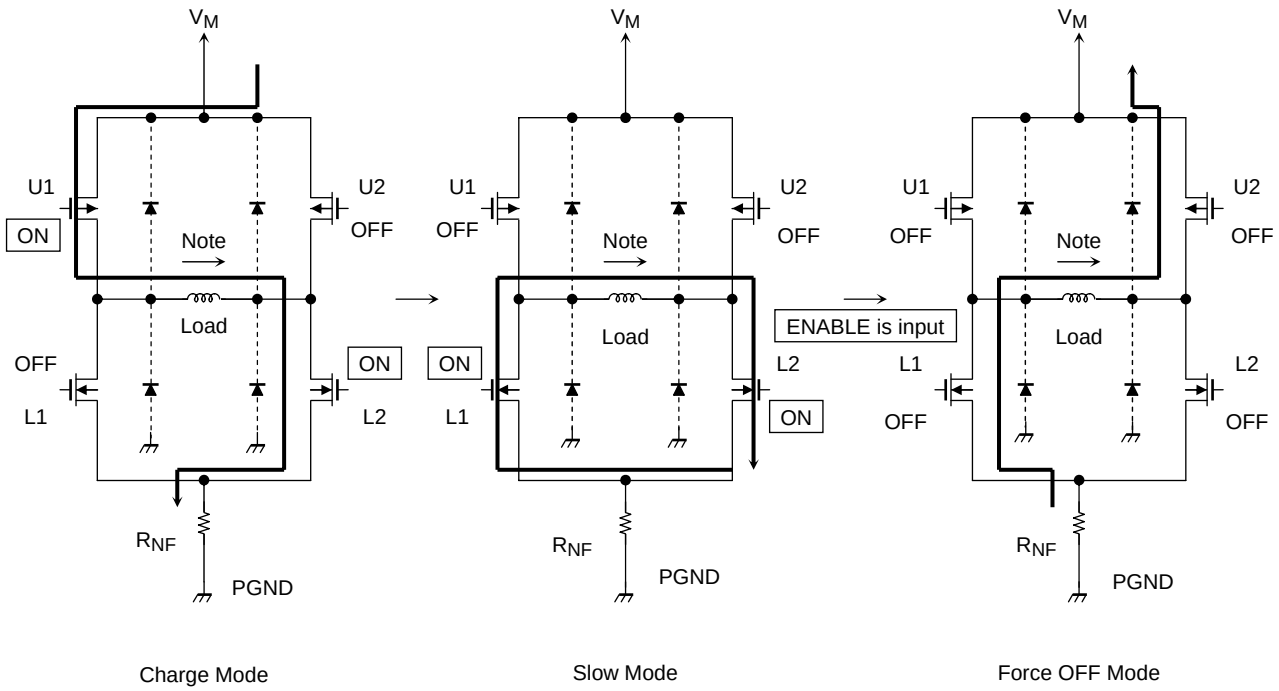
Current level

1/64, 1/32,1/16, 1/8,1/2	1/40, 1/20, 1/10	Min.	Typ.	Max.	Unit	1/64, 1/32,1/16, 1/8,1/2	1/40, 1/20, 1/10	Min.	Typ.	Max.	Unit
θ 64	θ 40	---	100.00	---		θ 30	---	63.2	67.16	71.2	
θ 63	θ 39	96.0	99.97	100.0		θ 29	θ 18	61.3	65.32	69.3	
θ 62	---	95.9	99.88	100.0		θ 28	---	59.4	63.44	67.4	
θ 61	θ 38	95.7	99.73	100.0		θ 27	θ 17	57.5	61.52	65.5	
θ 60	---	95.5	99.52	100.0		θ 26	---	55.6	59.57	63.6	
θ 59	θ 37	95.2	99.25	100.0		---	θ 16	54.8	58.78	62.8	
θ 58	θ 36	94.9	98.92	100.0		θ 25	---	53.6	57.58	61.6	
θ 57	---	94.5	98.53	100.0		θ 24	θ 15	51.6	55.56	59.6	
θ 56	θ 35	94.1	98.08	100.0		θ 23	---	49.5	53.50	57.5	
θ 55	---	93.6	97.57	100.0		---	θ 14	48.2	52.25	56.2	
θ 54	θ 34	93.0	97.00	100.0		θ 22	---	47.4	51.41	55.4	
θ 53	θ 33	92.4	96.38	100.0		θ 21	θ 13	45.3	49.29	53.3	
θ 52	---	91.7	95.69	99.7		θ 20	---	43.1	47.14	51.1	
θ 51	θ 32	91.0	94.95	99.0		θ 19	θ 12	41.0	44.96	49.0	
θ 50	θ 31	90.2	94.15	98.2		θ 18	---	38.8	42.76	46.8	
θ 49	---	89.3	93.30	97.3		---	θ 11	37.9	41.87	45.9	
θ 48	θ 30	88.4	92.39	96.4		θ 17	---	36.5	40.52	44.5	
θ 47	---	87.4	91.42	95.4		θ 16	θ 10	34.3	38.27	42.3	
---	θ 29	86.8	90.81	94.8		θ 15	---	32.0	35.99	40.0	
θ 46	---	86.4	90.40	94.4	%	---	θ 9	30.6	34.61	38.6	%
θ 45	θ 28	85.3	89.32	93.3		θ 14	---	29.7	33.69	37.7	
θ 44	---	84.2	88.19	92.2		θ 13	---	27.4	31.37	35.4	
θ 43	θ 27	83.0	87.01	91.0		---	θ 8	26.9	30.90	34.9	
θ 42	---	81.8	85.77	89.8		θ 12	---	25.0	29.03	33.0	
---	θ 26	81.3	85.26	89.3		θ 11	θ 7	22.7	26.67	30.7	
θ 41	---	80.5	84.49	88.5		θ 10	---	20.3	24.30	28.3	
θ 40	θ 25	79.1	83.15	87.1		---	θ 6	19.3	23.34	27.3	
θ 39	---	77.8	81.76	85.8		θ 9	---	17.9	21.91	25.9	
---	θ 24	76.9	80.90	84.9		θ 8	θ 5	15.5	19.51	23.5	
θ 38	---	76.3	80.32	84.3		θ 7	---	13.1	17.10	21.1	
θ 37	θ 23	74.8	78.83	82.8		---	θ 4	11.6	15.64	19.6	
θ 36	---	73.3	77.30	81.3		θ 6	---	10.7	14.67	18.7	
θ 35	θ 22	71.7	75.72	79.7		θ 5	θ 3	8.2	12.24	16.2	
θ 34	---	70.1	74.10	78.1		θ 4	---	5.8	9.80	13.8	
---	θ 21	69.4	73.43	77.4		θ 3	θ 2	3.4	7.36	11.4	
θ 33	---	68.4	72.42	76.4		θ 2	---	0.9	4.91	8.9	
θ 32	θ 20	66.7	70.71	74.7		---	θ 1	0.0	3.93	7.9	
θ 31	---	65.0	68.95	73.0		θ 1	---	0.0	2.45	6.5	
---	θ 19	63.9	67.88	71.9		θ 0	θ 0	---	0.0	---	

Current Draw-out Path when ENABLE is Input in Mid Operation

When all the output transistors are forced OFF during Slow mode, the coil energy is drawn out in the following modes:

Note: Parasitic diodes are indicated on the designed lines. However, these are not normally used in Mixed Decay mode.

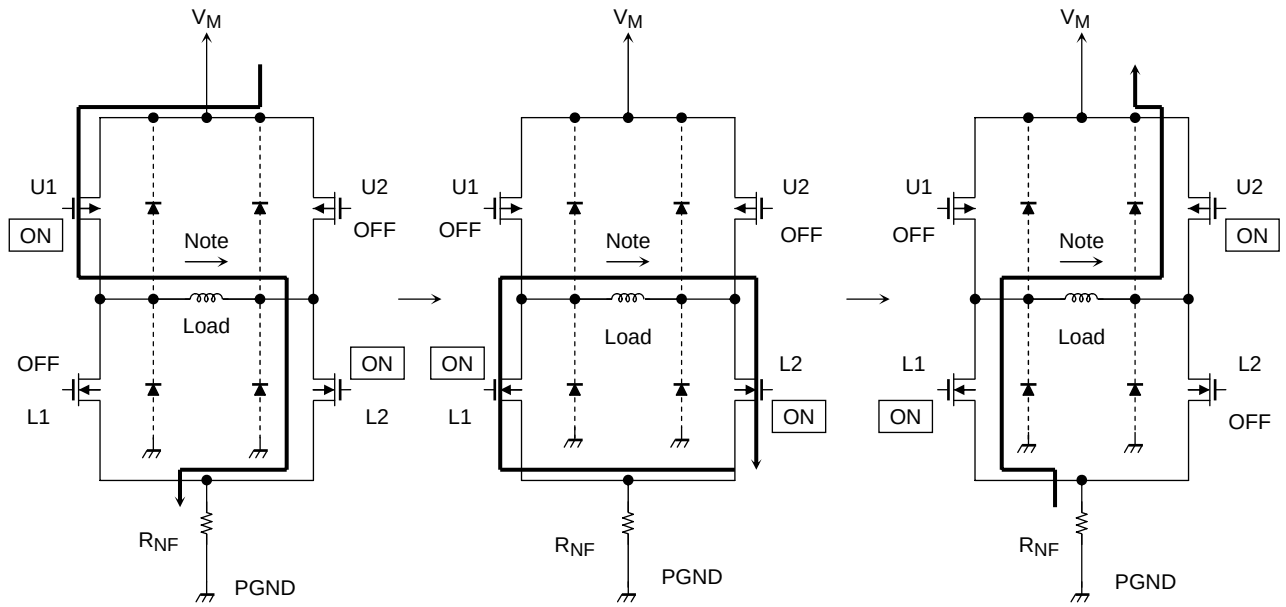


Charge Mode Slow Mode Force OFF Mode

As shown in the figure above, an output transistor has parasitic diodes.

Normally, when the energy of the coil is drawn out, each transistor is turned ON and the power flows in the opposite-to-normal direction; as a result, the parasitic diode is not used. However, when all the output transistors are forced OFF, the coil energy is drawn out via the parasitic diode.

Output Stage Transistor Operation Mode



Charge Mode Slow Mode Fast Mode

Output Stage Transistor Operation Functions

CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above chart shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following chart:

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Upon transitions of above-mentioned functions, a dead time of about 300 ns is inserted respectively.

Measurement Waveform

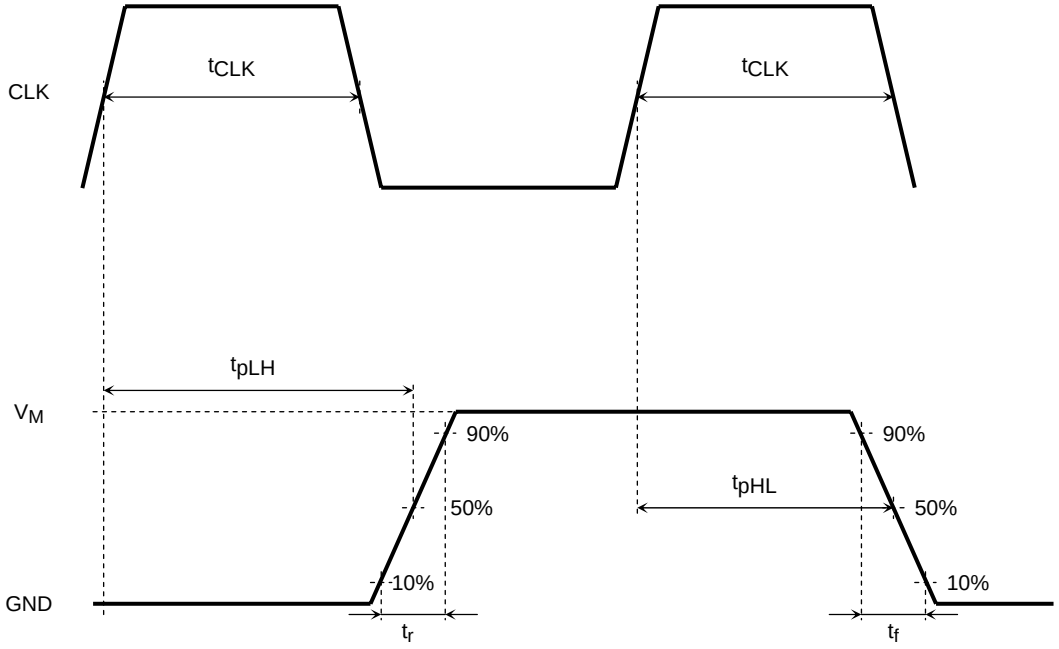
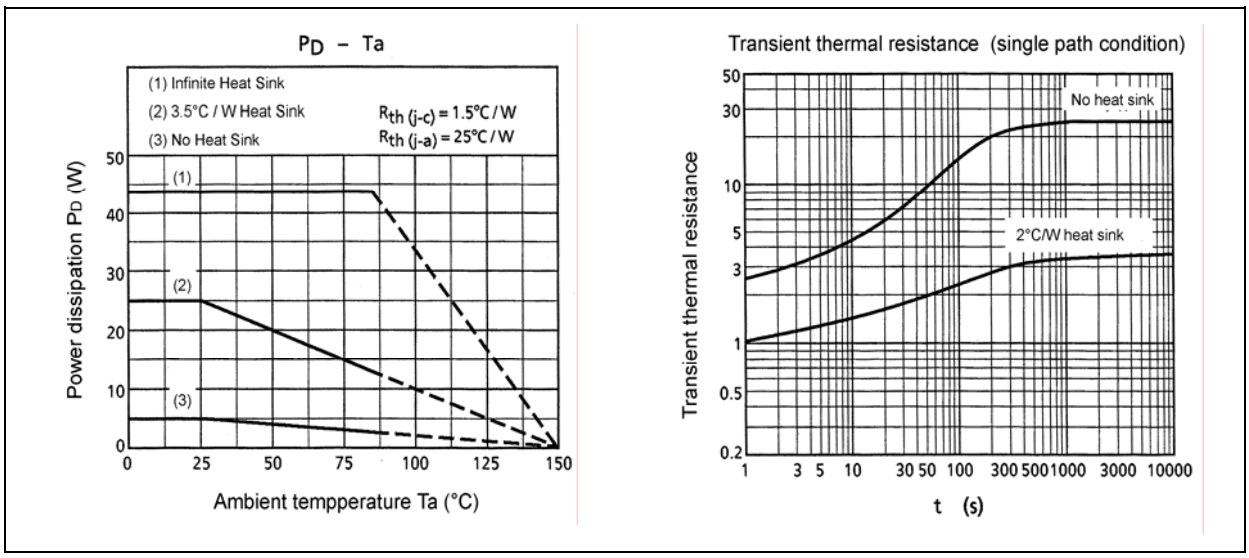


Figure 1 Timing Waveforms and Names

Power Dissipation

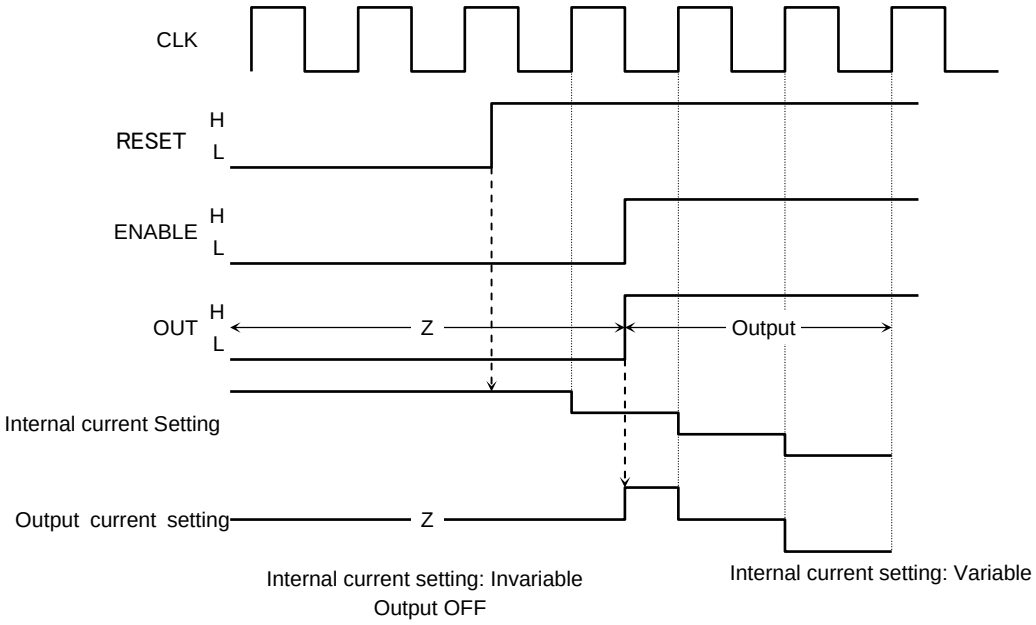
THB6064H



1. How to Turn on the Power

Turn on V_{DD}. When the voltage has stabilized, turn on $V_{MA/B}$.
In addition, set the Control Input pins to Low when inputting the power.
(All the Control Input pins are pulled down internally.)
Once the power is on, the CLK signal is received and excitation advances when RESET goes high and excitation is output when ENABLE goes high. If only RESET goes high, excitation won't be output and only the internal counter will advance. Likewise, if only ENABLE goes high, excitation won't advance even if the CLK signal is input and it will remain in the initial state.
The following is an example:

<Recommended Control Input Sequence>



2. Power Dissipation

The IC power dissipation is determined by the following equation:

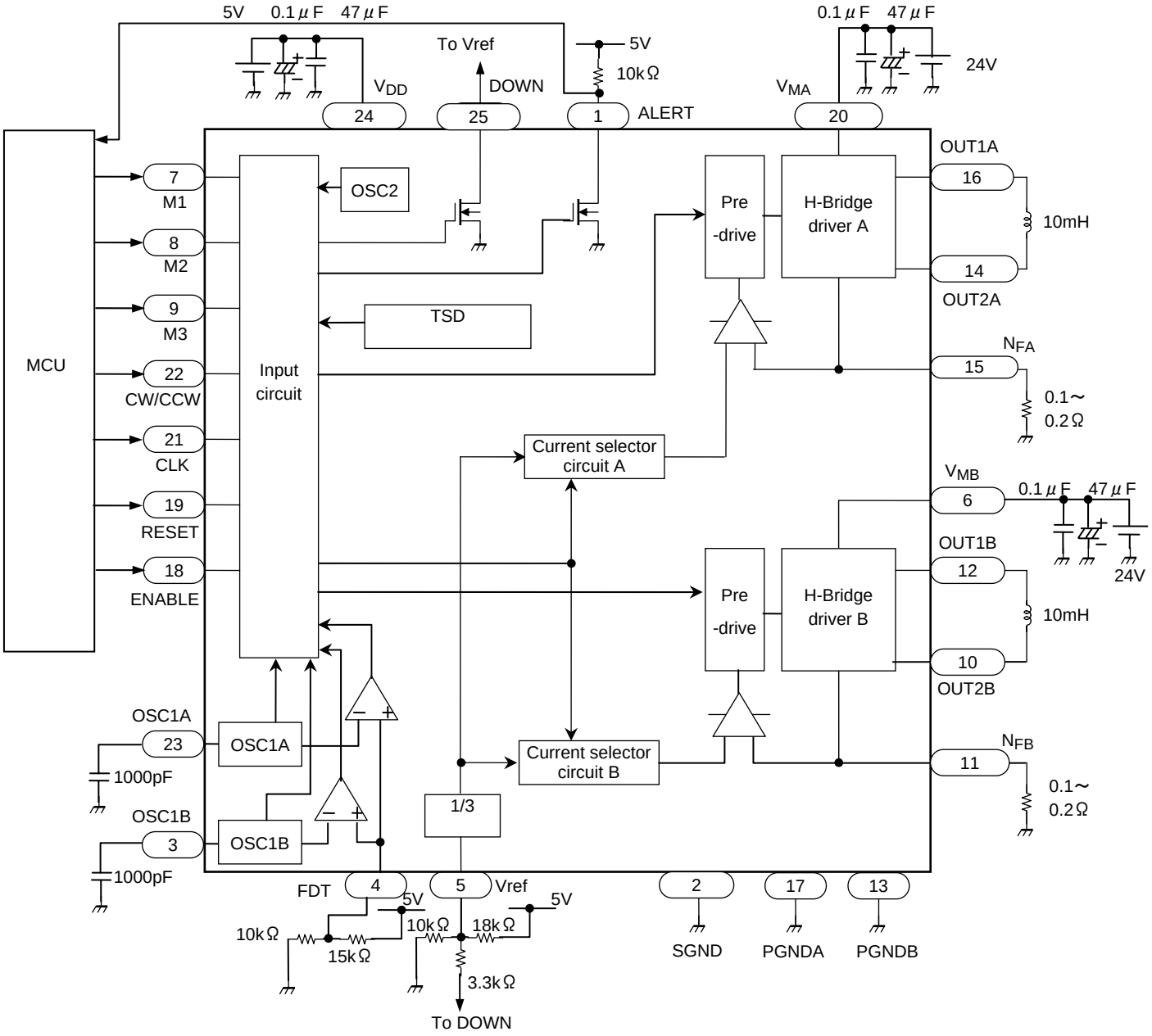
$P = V_{DD} \times I_{DD} + I_{OUT} \times I_{OUT}$ x Ron × 2 drivers

The higher the ambient temperature, the smaller the power dissipation.
Check the PD-Ta curve, and be sure to design the heat dissipation with a sufficient margin.

3. Heat Sink Fin Processing

The IC fin (rear) is electrically connected to the rear of the chip. If current flows to the fin, the IC will malfunction. If there is any possibility of a voltage being generated between the IC GND and the fin, either ground the fin or insulate it.

Application example



Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics.
These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

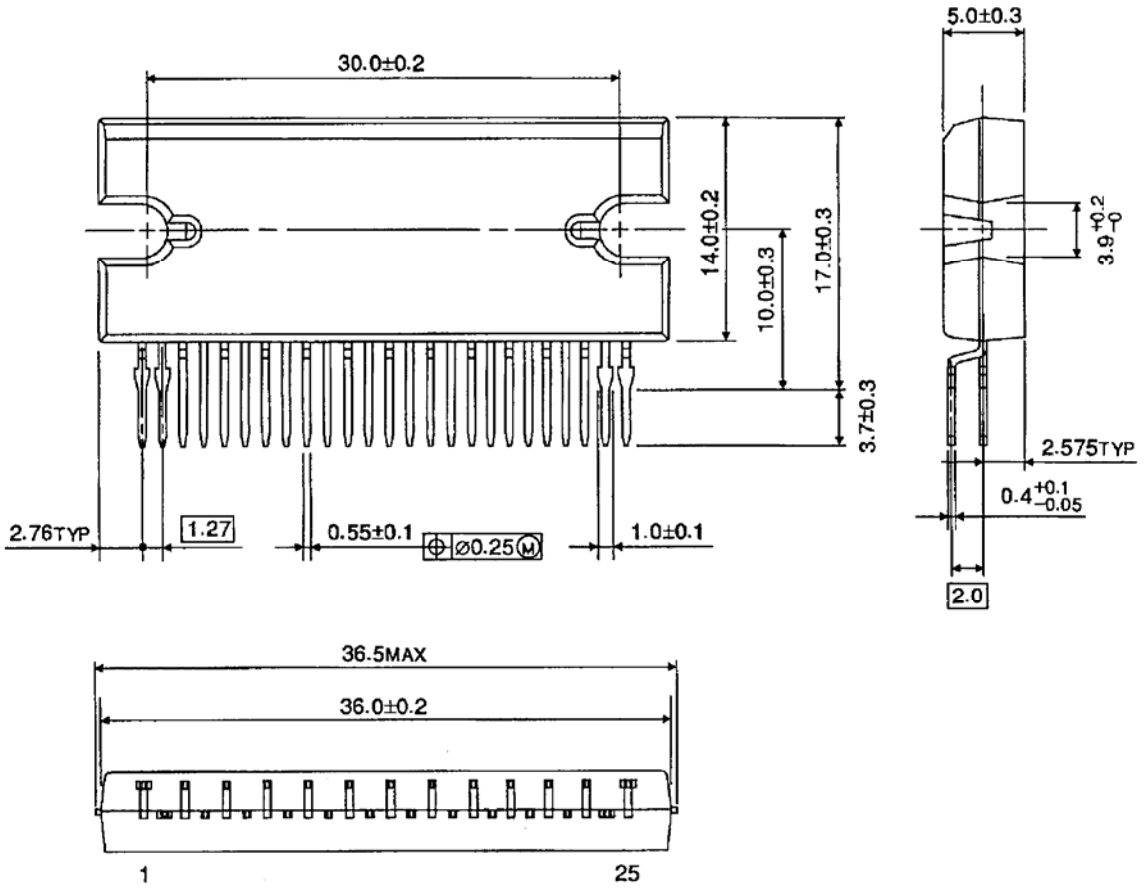
[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Package Dimensions

HZIP25-P-1.27 Unit : mm



Weight: 9.86 g (typ.)